

COMPAL CONFIDENTIAL

MODEL NAME : QAR10

PCB NO : LA-7933P

BOM P/N : 4319FV31L01

GPIO MAP: E4 VC GPIO map rev 1.1

Vans 17

REV : 0.2 (X01)

2011.11.11

@ : Nopop Component

CONN@ : Connector Component

PXDP@: PCH XDP Component

MB Type	BOM P/N		
TPM EN/ TCM DIS		1@	3@
TPM DIS/ TCM EN		2@	3@
TPM DIS/ TCM DIS		2@	4@

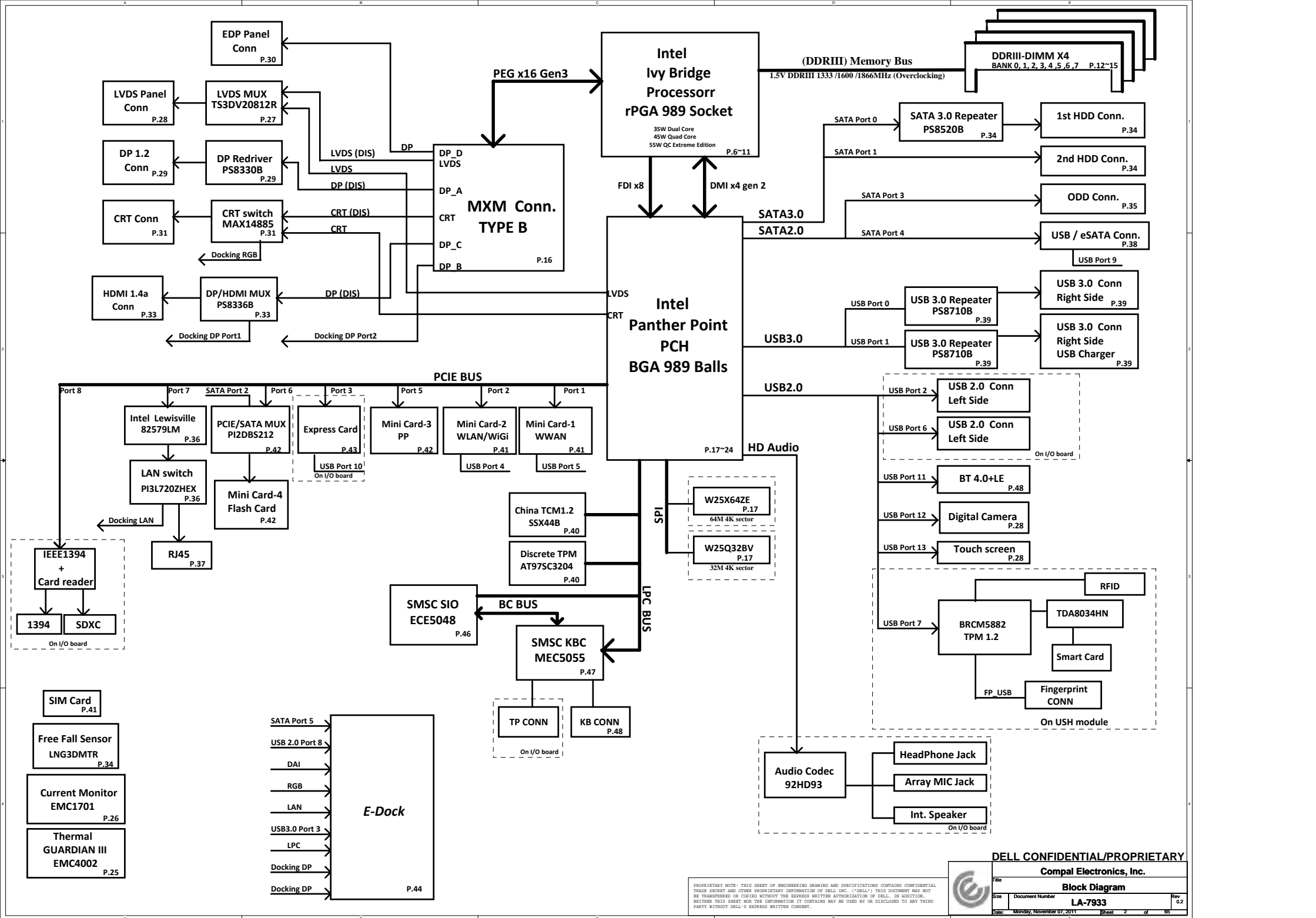
MB PCB	
Part Number	Description
DAA00002U00	PCB OMF LA-7933P REVO MB

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top		Copper foil	0.5oz
		3.7	Prepreg	1080
2	Core 1		Copper foil	1oz
		3.7	Core	4mil
3	Sig 1		Copper foil	1oz
		3.9	Prepreg	1080H+2116H
4	Core/PWR		Copper foil	2oz
		3.7	Core	4mil
5	Sig 2		Copper foil	1oz
		3.8	Prepreg	1080Hx2
6	Sig 3		Copper foil	1oz
		3.7	Core	4mil
7	Core/PWR		Copper foil	2oz
		3.9	Prepreg	1080H+2116H
8	Sig 4		Copper foil	1oz
		3.7	Core	4mil
9	Core 3		Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	57.09
Overall Thickness (1.45mm ± 10%)				

SATA	DESTINATION
SATA 0	HDD 1
SATA 1	HDD 2
SATA 2	NVRAM
SATA 3	ODD
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side)
	1	JUSB2 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	WLAN
	5	WWAN
	6	IO Board- JUSB2 (Ext Left Side)
	7	USH
	8	Docking USB 2.0
	9	ESATA
	10	Express Card
	11	BT 4.0
	12	Carmera
	13	Touch Screen

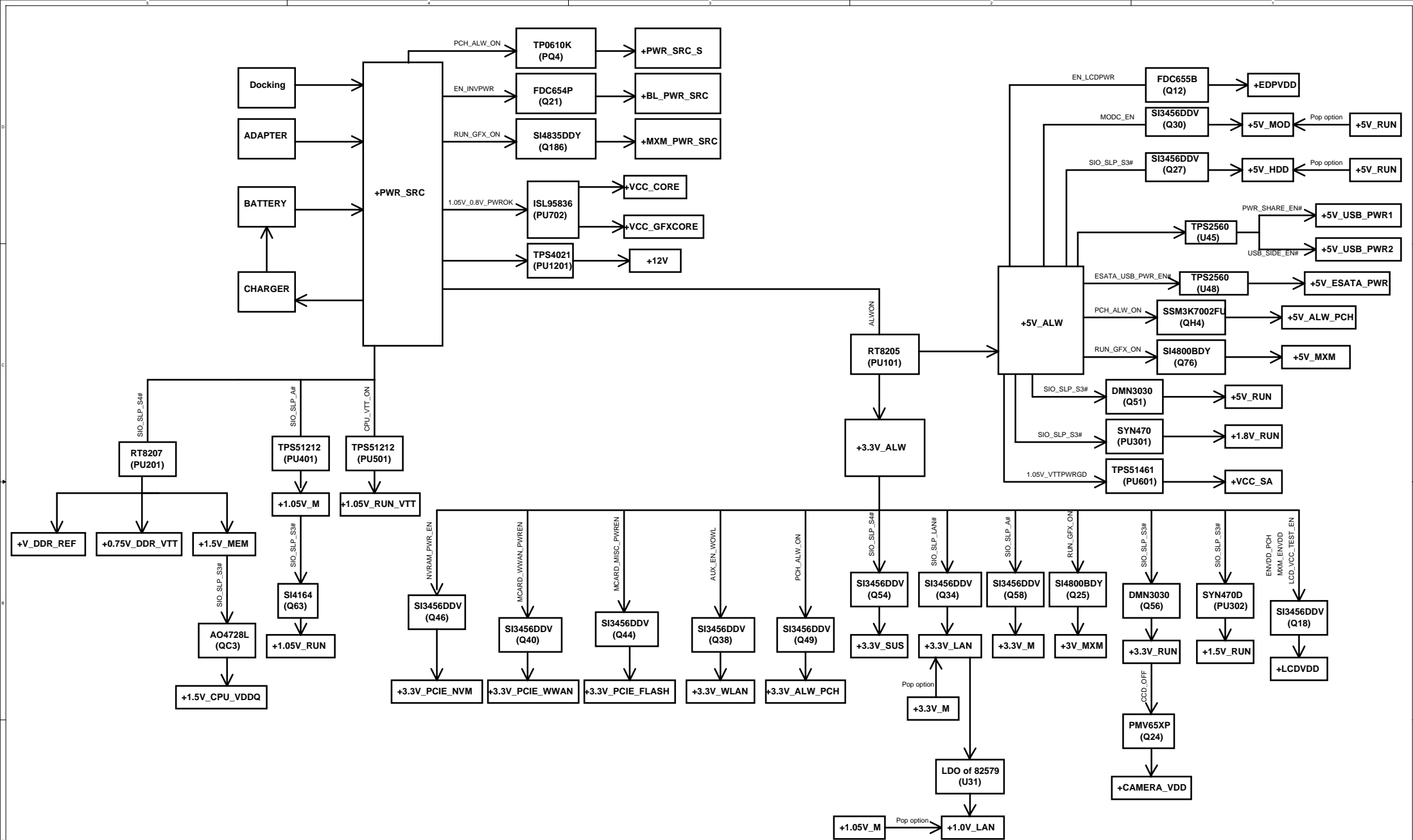
USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express Card
Lane 4	NA
Lane 5	MINI CARD-3 (Pink Panther)
Lane 6	NVRAM Card
Lane 7	10/100/1G LOM
Lane 8	Cardreader

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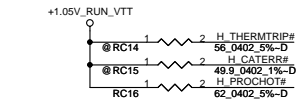
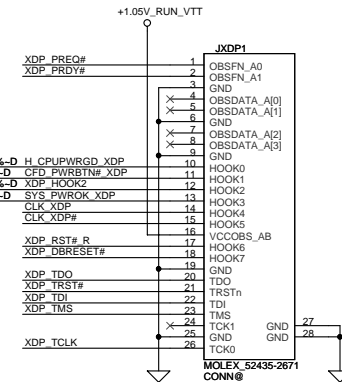
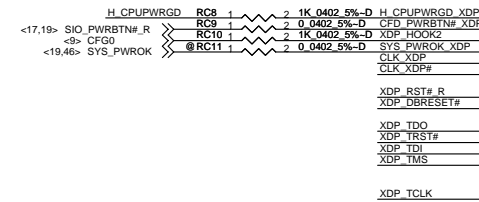
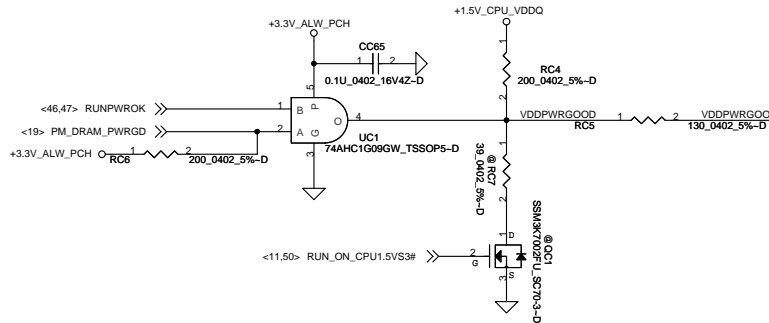


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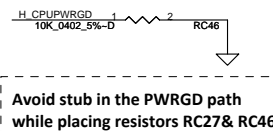
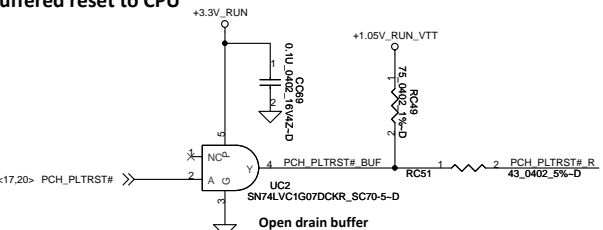
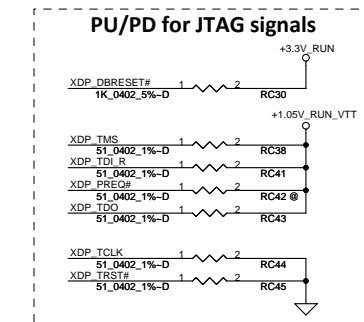
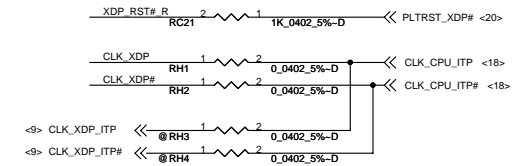
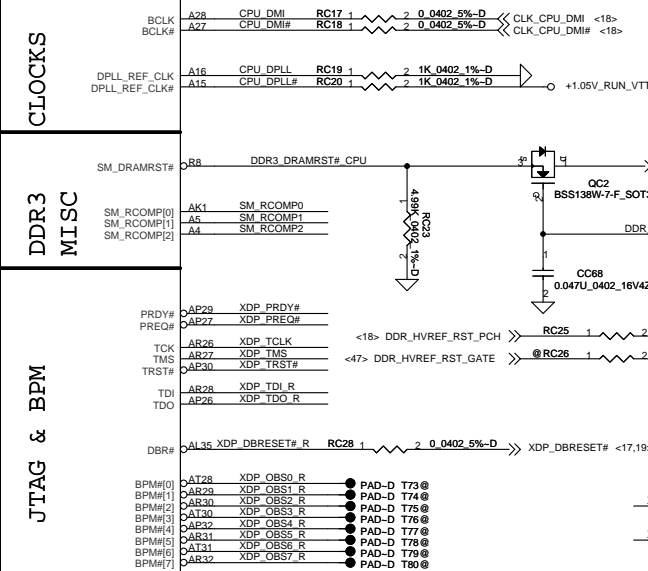
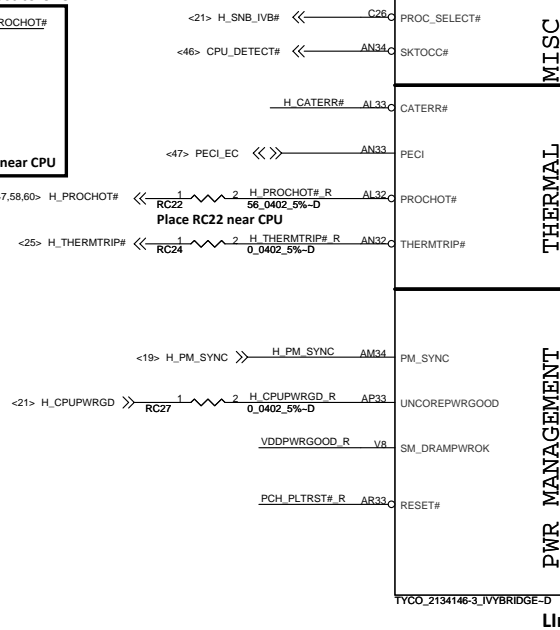
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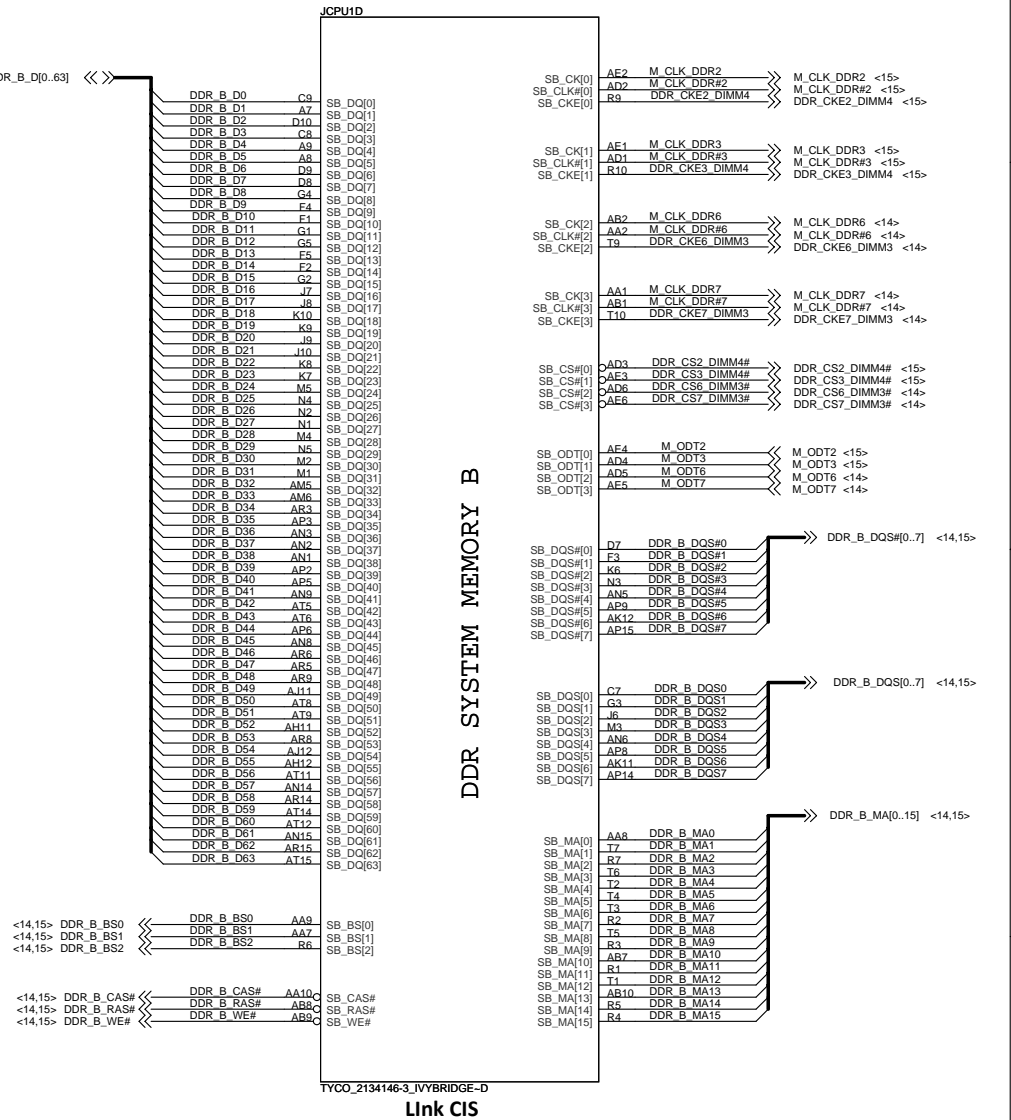
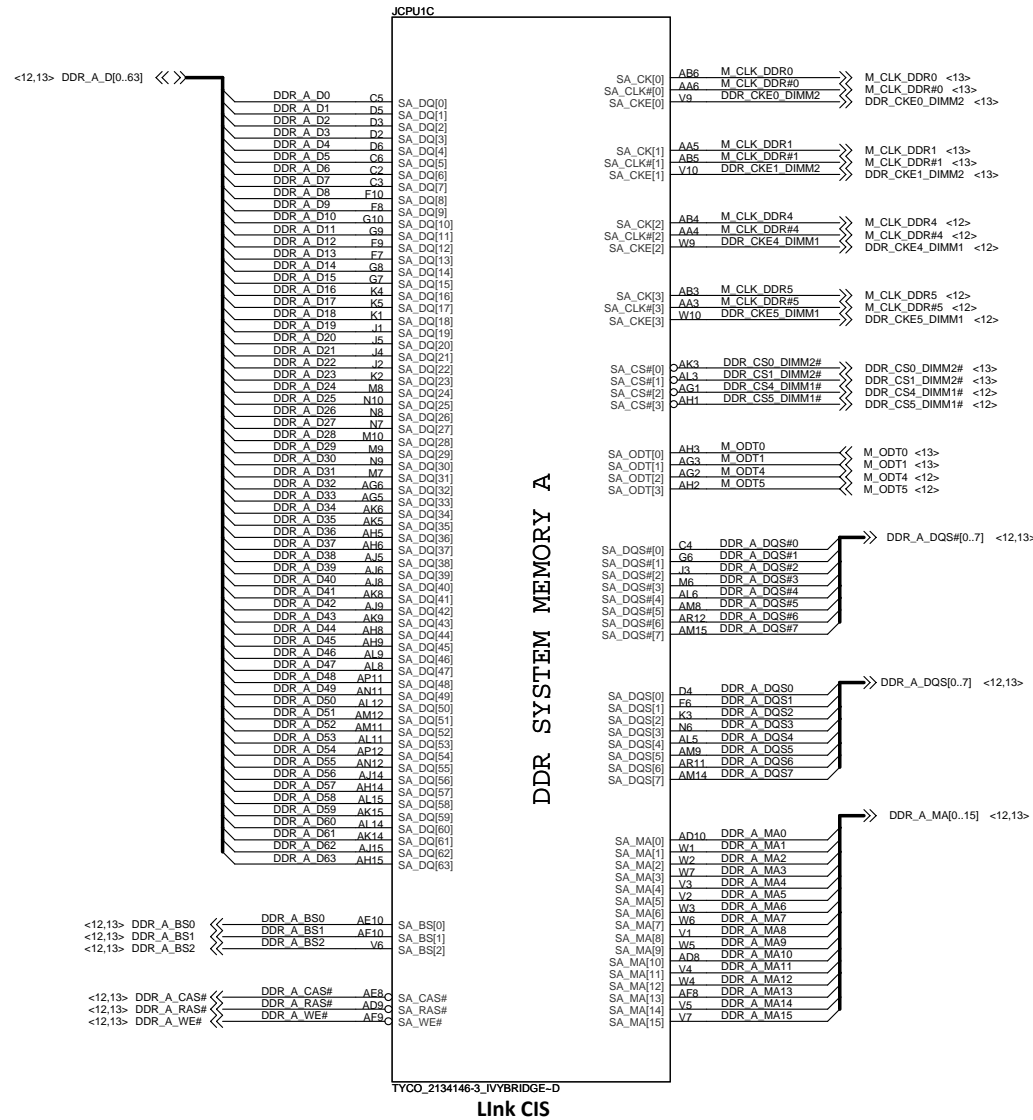
H_PROCHOT#

CC92
220P 0402 50V7K-D

Place CC92 near CPU



SM RCOMP2	1	2	RC47
200_0402_1%-D			
SM RCOMP1	1	2	RC48
25.5_0402_1%-D			
SM RCOMP0	1	2	RC50
140_0402_1%-D			



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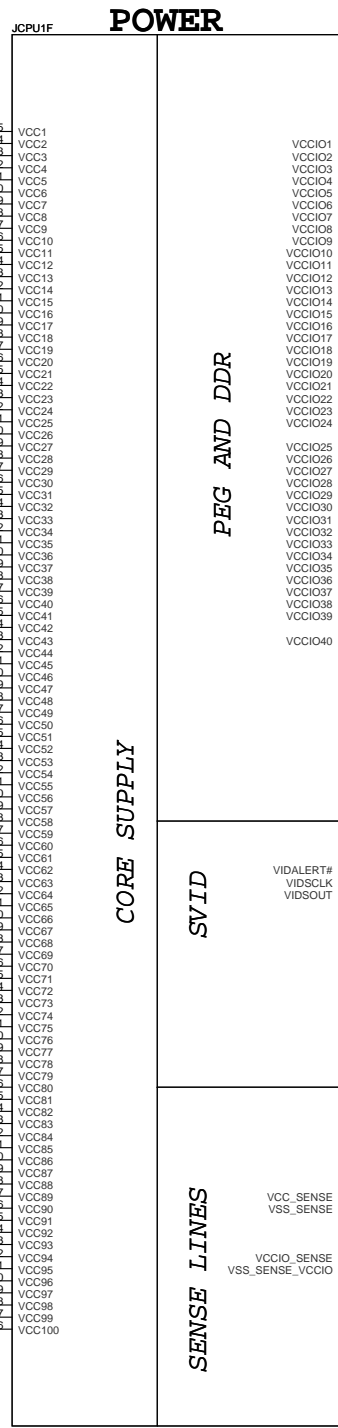
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Ivy Bridge (3/6)

LA-7933

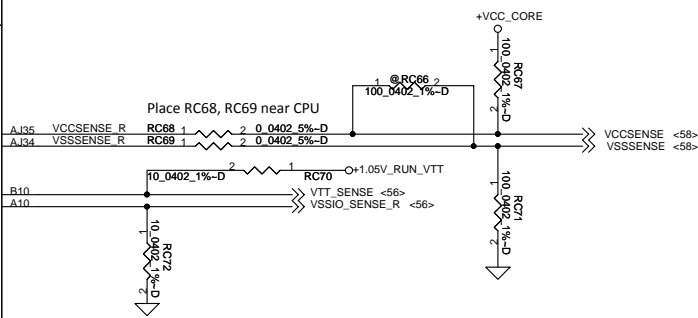
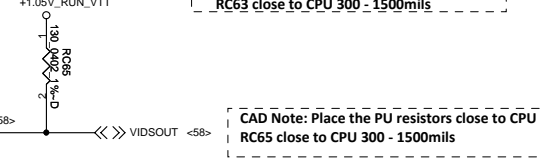
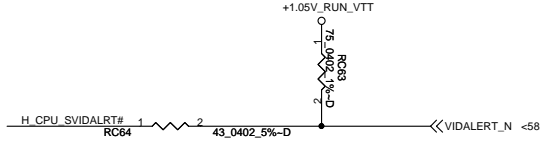
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Ivy Bridge (3/6)		0.2	
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TYCO_2134146-3_IVYBRIDGE-D

Link CIS



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[illegible]

The schematic diagram illustrates the power supply and sense lines for the JCPU1G1G. It shows connections for VCC_GFXCORE, VAXG1 through VAXG12, VAXG_SENSE, VSSAXG_SENSE, SM_VREF, and +V_SM_VREF_CNT. The diagram includes components like resistors (R34, R35, R36), capacitors (C1, C2), and a voltage divider network (RC85, RC86).

GRAPHICS

-1.5V RAILS

VREF

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ

Checking again

5A

6A

+1.5V_CPU_VDDQ

+1.5V_MEM

AP23 VAXG13
AP21 VAXG14
AP20 VAXG15
AP18 VAXG16
AP17 VAXG17
AP16 VAXG18
AN24 VAXG19
AN23 VAXG20
AN21 VAXG21
AN20 VAXG22
AN18 VAXG23
AN17 VAXG24
AM24 VAXG25
AM23 VAXG26
AM21 VAXG27
AM20 VAXG28
AM18 VAXG29
AM17 VAXG30
AL24 VAXG31
AL23 VAXG32
AL21 VAXG33
AL20 VAXG34
AL18 VAXG35
AL17 VAXG36
AK24 VAXG37
AK23 VAXG38
AK21 VAXG39

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 ACZ
VDDQ5 ACZ
VDDQ6 AC4
VDDQ7 AC1
VDDQ8 Y7
VDDQ9 Y4
VDDQ10 Y1
VDDQ11 U7
VDDQ12 U4
VDDQ13 J1
VDDQ14 P7
VDDQ15 P4
VDDQ16 P1

CC75 10.0603, 6.3V6M-D
CC76 10.0603, 6.3V6M-D
CC77 10.0603, 6.3V6M-D
CC78 10.0603, 6.3V6M-D
CC79 10.0603, 6.3V6M-D
CC80 10.0603, 6.3V6M-D
CC81 10.0603, 6.3V6M-D
CC82 10.0603, 6.3V6M-D
CC83 10.0603, 6.3V6M-D
CC84 10.0603, 6.3V6M-D
CC85 10.0603, 6.3V6M-D
CC86 10.0603, 6.3V6M-D
CC87 10.0603, 6.3V6M-D
CC88 10.0603, 6.3V6M-D
CC89 10.0603, 6.3V6M-D
CC90 10.0603, 6.3V6M-D
CC91 10.0603, 6.3V6M-D
CC92 10.0603, 6.3V6M-D
CC93 10.0603, 6.3V6M-D
CC94 10.0603, 6.3V6M-D
CC95 10.0603, 6.3V6M-D
CC96 10.0603, 6.3V6M-D
CC97 10.0603, 6.3V6M-D
CC98 10.0603, 6.3V6M-D
CC99 10.0603, 6.3V6M-D
CC100 10.0603, 6.3V6M-D
CC101 10.0603, 6.3V6M-D
CC102 10.0603, 6.3V6M-D
CC103 10.0603, 6.3V6M-D
CC104 10.0603, 6.3V6M-D
CC105 10.0603, 6.3V6M-D
CC106 10.0603, 6.3V6M-D
CC107 10.0603, 6.3V6M-D
CC108 10.0603, 6.3V6M-D
CC109 10.0603, 6.3V6M-D
CC110 10.0603, 6.3V6M-D
CC111 10.0603, 6.3V6M-D
CC112 10.0603, 6.3V6M-D
CC113 10.0603, 6.3V6M-D
CC114 10.0603, 6.3V6M-D
CC115 10.0603, 6.3V6M-D
CC116 10.0603, 6.3V6M-D
CC117 10.0603, 6.3V6M-D
CC118 10.0603, 6.3V6M-D
CC119 10.0603, 6.3V6M-D
CC120 10.0603, 6.3V6M-D
CC121 10.0603, 6.3V6M-D
CC122 10.0603, 6.3V6M-D
CC123 10.0603, 6.3V6M-D
CC124 10.0603, 6.3V6M-D
CC125 10.0603, 6.3V6M-D
CC126 10.0603, 6.3V6M-D
CC127 10.0603, 6.3V6M-D
CC128 10.0603, 6.3V6M-D
CC129 10.0603, 6.3V6M-D
CC130 10.0603, 6.3V6M-D
CC131 10.0603, 6.3V6M-D
CC132 10.0603, 6.3V6M-D
CC133 10.0603, 6.3V6M-D
CC134 10.0603, 6.3V6M-D
CC135 10.0603, 6.3V6M-D
CC136 10.0603, 6.3V6M-D
CC137 10.0603, 6.3V6M-D
CC138 10.0603, 6.3V6M-D
CC139 10.0603, 6.3V6M-D
CC140 10.0603, 6.3V6M-D
CC141 10.0603, 6.3V6M-D
CC142 10.0603, 6.3V6M-D
CC143 10.0603, 6.3V6M-D
CC144 10.0603, 6.3V6M-D
CC145 10.0603, 6.3V6M-D
CC146 10.0603, 6.3V6M-D
CC147 10.0603, 6.3V6M-D
CC148 10.0603, 6.3V6M-D
CC149 10.0603, 6.3V6M-D
CC150 10.0603, 6.3V6M-D
CC151 10.0603, 6.3V6M-D
CC152 10.0603, 6.3V6M-D
CC153 10.0603, 6.3V6M-D
CC154 10.0603, 6.3V6M-D
CC155 10.0603, 6.3V6M-D
CC156 10.0603, 6.3V6M-D
CC157 10.0603, 6.3V6M-D
CC158 10.0603, 6.3V6M-D
CC159 10.0603, 6.3V6M-D
CC160 10.0603, 6.3V6M-D
CC161 10.0603, 6.3V6M-D
CC162 10.0603, 6.3V6M-D
CC163 10.0603, 6.3V6M-D
CC164 10.0603, 6.3V6M-D
CC165 10.0603, 6.3V6M-D
CC166 10.0603, 6.3V6M-D
CC167 10.0603, 6.3V6M-D
CC168 10.0603, 6.3V6M-D
CC169 10.0603, 6.3V6M-D
CC170 10.0603, 6.3V6M-D
CC171 10.0603, 6.3V6M-D
CC172 10.0603, 6.3V6M-D
CC173 10.0603, 6.3V6M-D
CC174 10.0603, 6.3V6M-D
CC175 10.0603, 6.3V6M-D
CC176 10.0603, 6.3V6M-D
CC177 10.0603, 6.3V6M-D
CC178 10.0603, 6.3V6M-D
CC179 10.0603, 6.3V6M-D
CC180 10.0603, 6.3V6M-D
CC181 10.0603, 6.3V6M-D
CC182 10.0603, 6.3V6M-D
CC183 10.0603, 6.3V6M-D
CC184 10.0603, 6.3V6M-D
CC185 10.0603, 6.3V6M-D
CC186 10.0603, 6.3V6M-D
CC187 10.0603, 6.3V6M-D
CC188 10.0603, 6.3V6M-D
CC189 10.0603, 6.3V6M-D
CC190 10.0603, 6

[illegible]

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AT35			AJ22
AT32	VSS1	VSS81	A119
VSS3	VSS2	VSS82	A116
AT27	VSS3	VSS83	A113
AT25	VSS4	VSS84	A110
AT22	VSS5	VSS85	A17
VSS6	VSS6	VSS86	A14
AT19	VSS7	VSS87	A12
AT16	VSS8	VSS88	A1
AT13	VSS9	VSS89	AH35
AT10	VSS10	VSS90	AH34
AT7	VSS11	VSS91	AH32
AT4	VSS12	VSS92	AH30
AT3	VSS13	VSS93	AH29
AR25	VSS14	VSS94	AH28
AR22	VSS15	VSS95	AH25
AR19	VSS16	VSS96	AH22
AR16	VSS17	VSS98	AH19
AR13	VSS18	VSS99	AH16
AR10	VSS19	VSS100	AH7
AR7	VSS20	VSS101	AH4
AR4	VSS21	VSS102	AG9
AR2	VSS22	VSS103	AG8
AP34	VSS23	VSS104	AG4
AP31	VSS24	VSS105	AF6
AP28	VSS25	VSS106	AF5
AP25	VSS26	VSS107	AF3
AP22	VSS27	VSS108	AF2
AP19	VSS28	VSS109	AE35
AP16	VSS29	VSS110	AE34
AP13	VSS30	VSS111	AE33
AP10	VSS31	VSS112	AE32
AP7	VSS32	VSS113	AE31
AP4	VSS33	VSS114	AE30
AP1	VSS34	VSS115	AE29
AN30	VSS35	VSS116	AE28
AN27	VSS36	VSS117	AE27
AN25	VSS37	VSS118	AE26
AN22	VSS38	VSS119	AE9
AN19	VSS39	VSS120	AD7
AN16	VSS40	VSS121	AC9
AN13	VSS41	VSS122	AC8
AN10	VSS42	VSS123	AC6
AN7	VSS43	VSS124	AC5
AN4	VSS44	VSS125	AC4
AM28	VSS45	VSS126	AC2
AM25	VSS46	VSS127	AB35
AM22	VSS47	VSS128	AB34
AM19	VSS48	VSS129	AB33
AM16	VSS49	VSS130	AB32
AM13	VSS50	VSS131	AB31
AM10	VSS51	VSS132	AB30
AM7	VSS52	VSS133	AB29
AM4	VSS53	VSS134	AB28
AM3	VSS54	VSS135	AB27
AM2	VSS55	VSS136	AB26
AM1	VSS56	VSS137	Y9
AL34	VSS57	VSS138	Y8
AL31	VSS58	VSS139	Y6
AL28	VSS59	VSS140	Y5
AL25	VSS60	VSS141	Y3
AL22	VSS61	VSS142	Y2
AL19	VSS62	VSS143	W35
AL16	VSS63	VSS144	W34
AL13	VSS64	VSS145	W33
AL10	VSS65	VSS146	W32
AL7	VSS66	VSS147	W31
AL4	VSS67	VSS148	W30
AL2	VSS68	VSS149	W29
AK33	VSS69	VSS150	W28
AK30	VSS70	VSS151	W27
AK27	VSS71	VSS152	W26
AK25	VSS72	VSS153	U9
AK22	VSS73	VSS154	U8
AK19	VSS74	VSS155	U6
AK16	VSS75	VSS156	U5
AK13	VSS76	VSS157	U3
AK10	VSS77	VSS158	U2
AK7	VSS78	VSS159	
AK4	VSS79	VSS160	
AP25	VSS80		

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	Title	Ivy Bridge (6/6)
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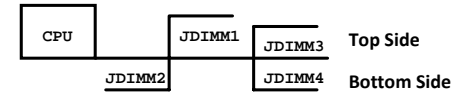
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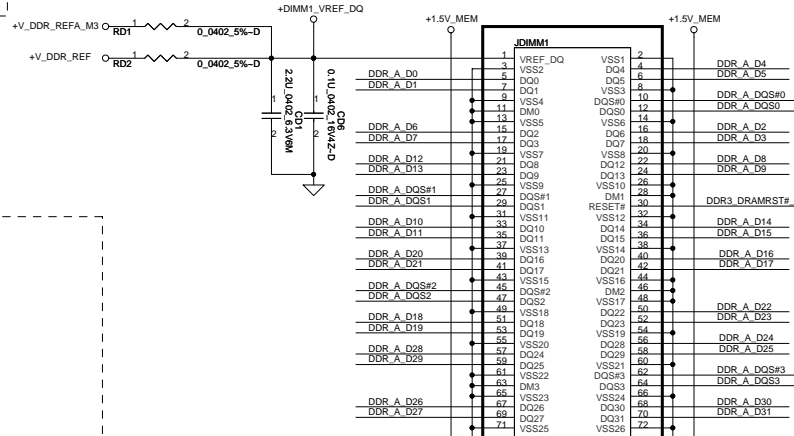
All VREF traces should have 10 mil trace width

Populate RD1, De-Populate RD2 for Intel DDR3
VREFDQ multiple methods M1
Populate RD2, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3

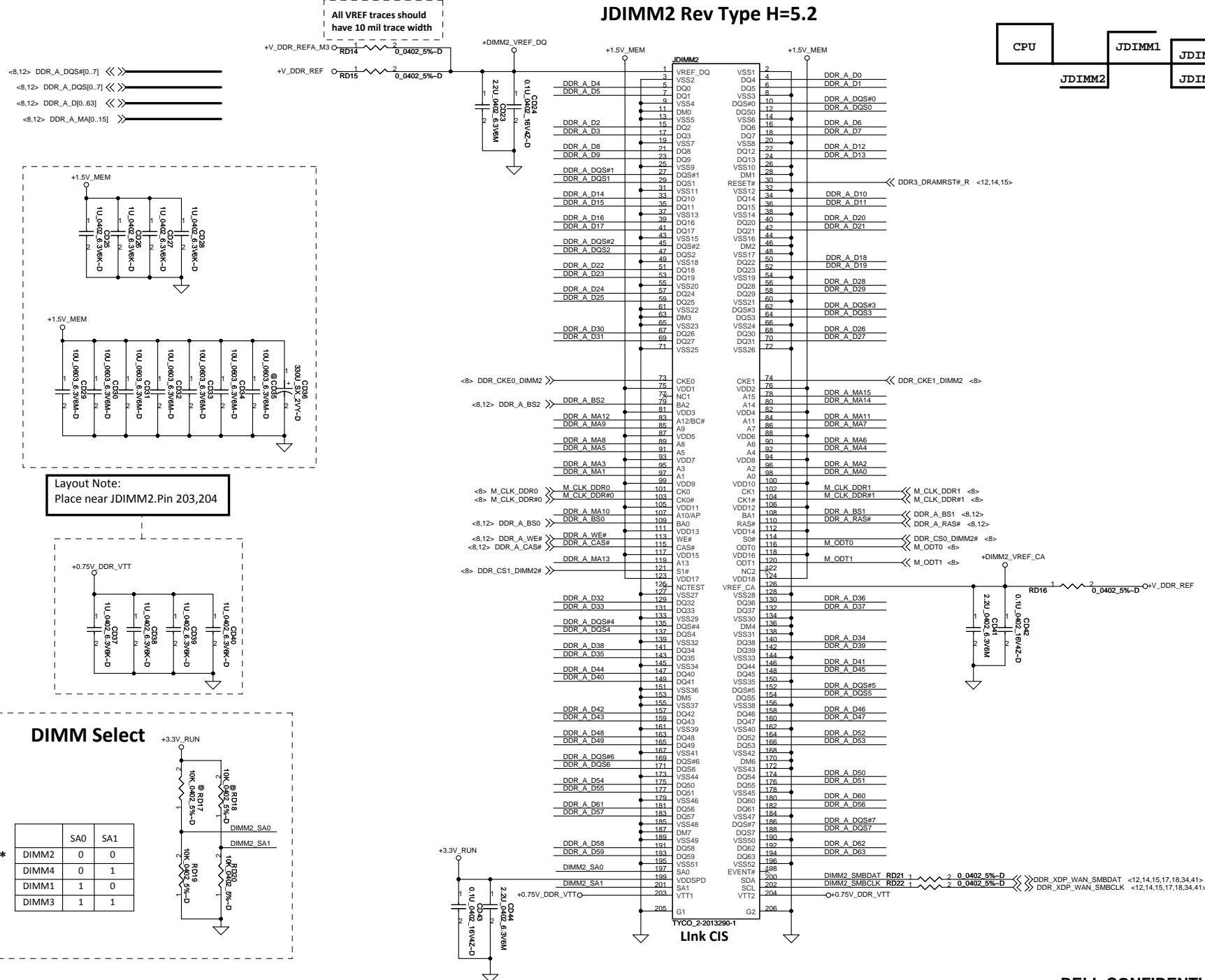
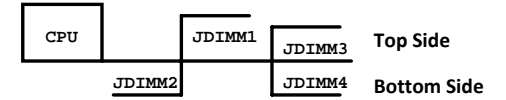
JDIMM1 Rev Type H=9.2



<8.13> DDR_A_DQS#0[0..7] <<>
<8.13> DDR_A_DQS#0[0..7] <<>
<8.13> DDR_A_D[0..63] <<>
<8.13> DDR_A_MA[0..15] <<>



JDIMM2 Rev Type H=5.2



Layout Note:
Place near JDIMM2.Pin 203,204

DIMM Select

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1

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DDR3-SODIMM SLOT2

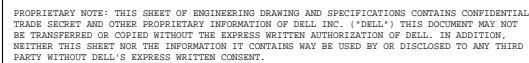
LA-7933

Date: Monday, November 07, 2011 Sheet: 13 of 85

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Diagram illustrating the component layout on the top and bottom sides of the board:

- Top Side:** CPU, JDIMM1, JDIMM3
- Bottom Side:** JDIMM2, JDIMM4



Title			DDRIII-SODIMM SLOT3		
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```
<8,14> DDR_B_DQS#[0..7] << >>
<8,14> DDR_B_DQS[0..7] << >>
<8,14> DDR_B_D[0..63] << >>
<8,14> DDR_B_MA[0..15] >>
```

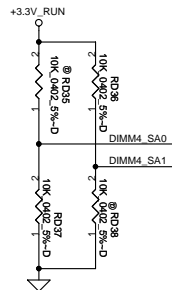
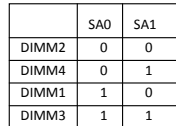
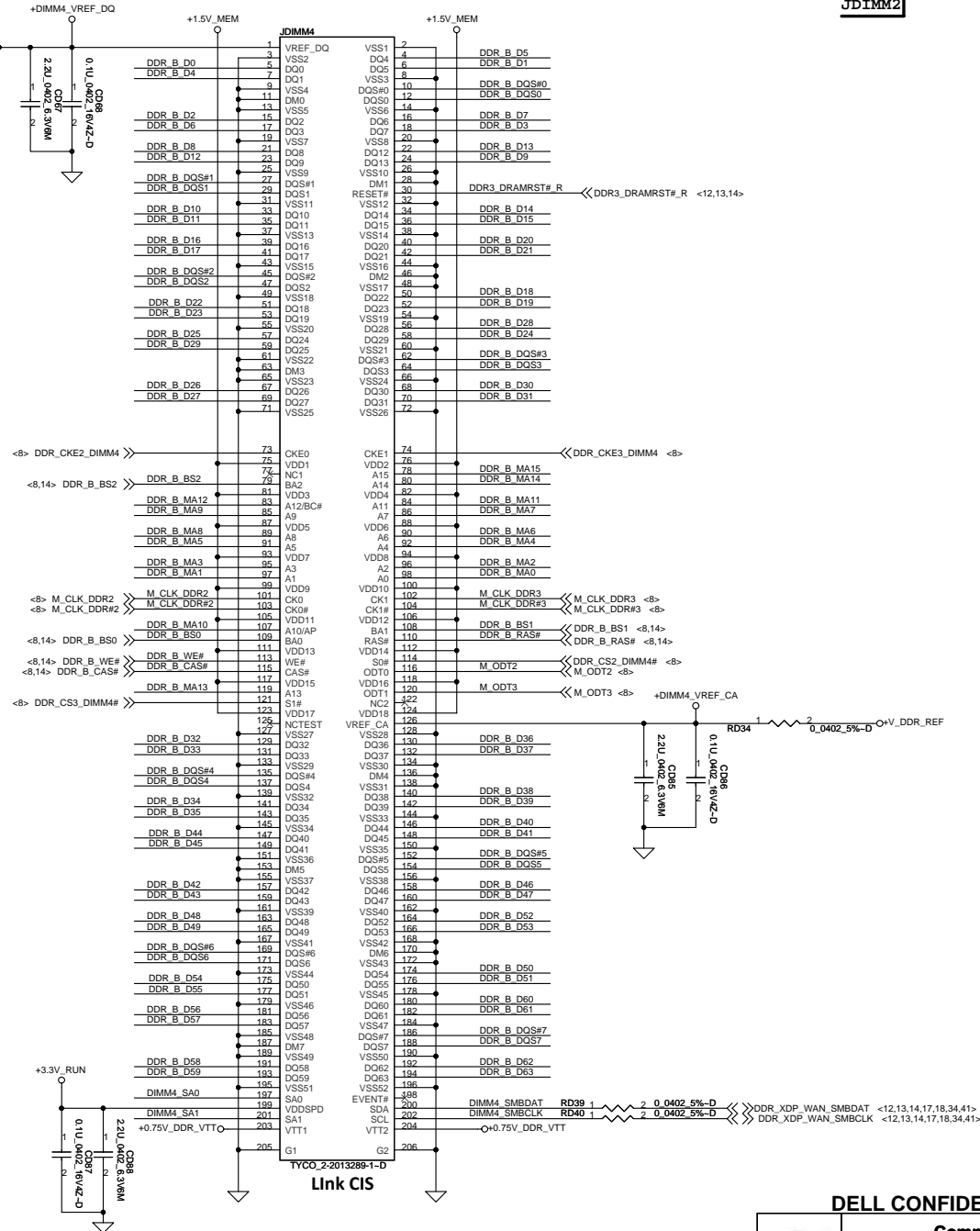


Diagram illustrating the board layout components:

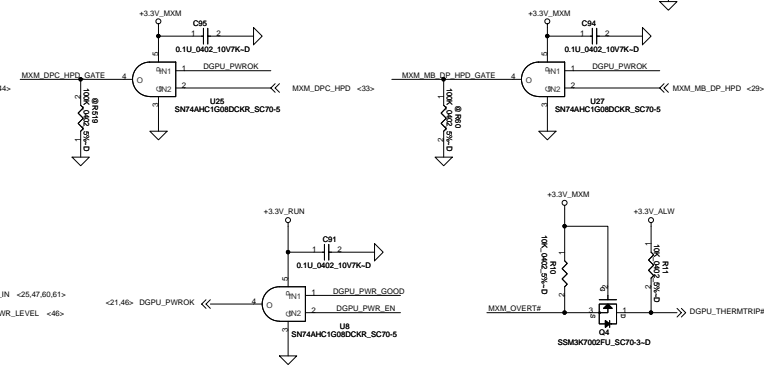
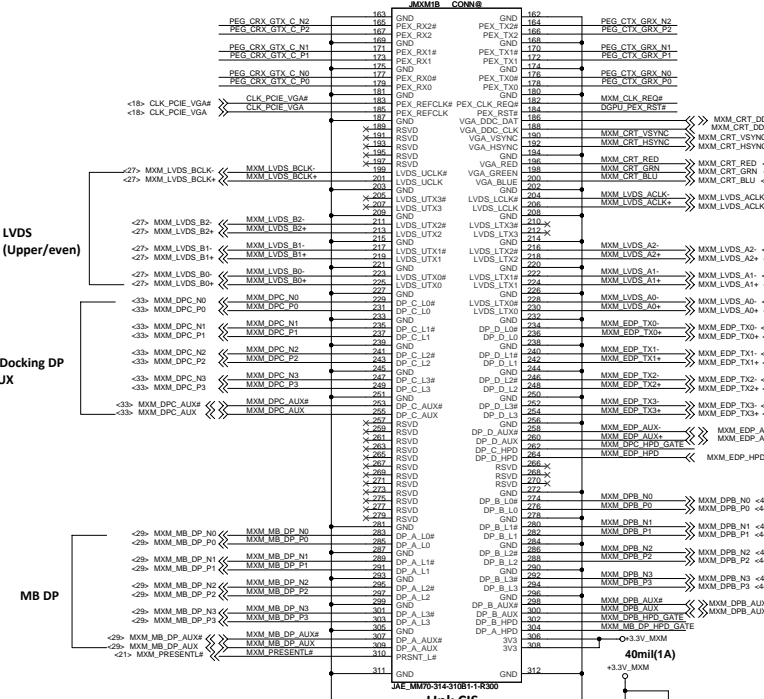
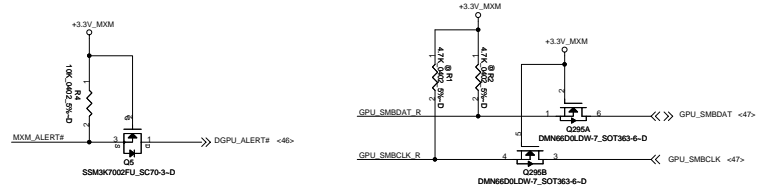
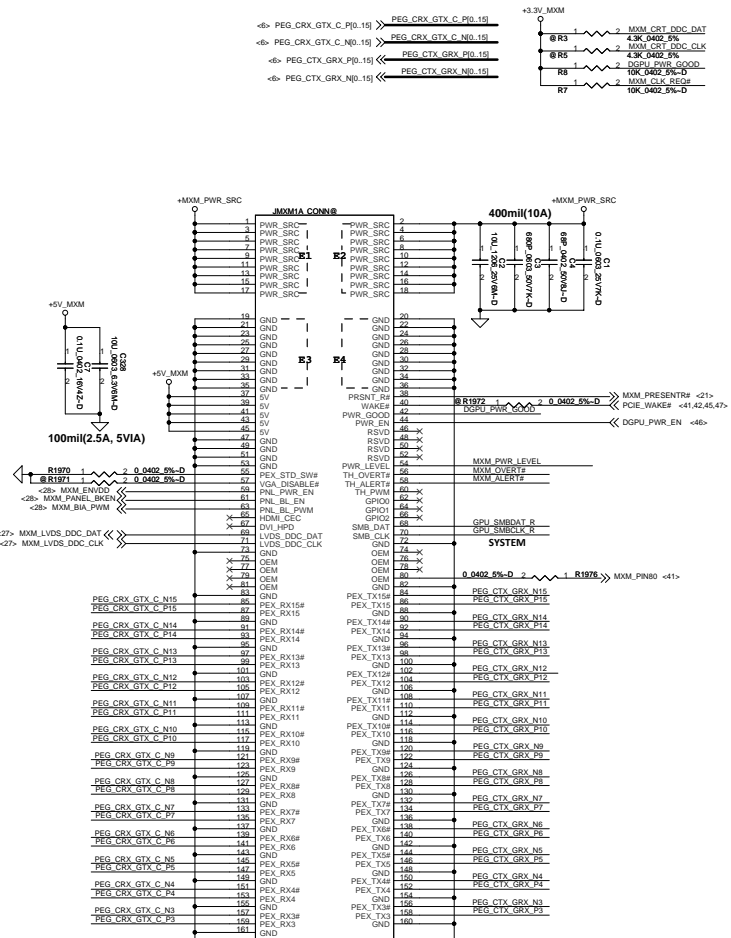
- Top Side:** CPU, JDIMM1, JDIMM3
- Bottom Side:** JDIMM2, JDIMM4



Rev	0.2
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CRT
LVDS (Lower/odd)
eDP
Docking DP port 2

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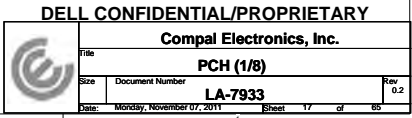
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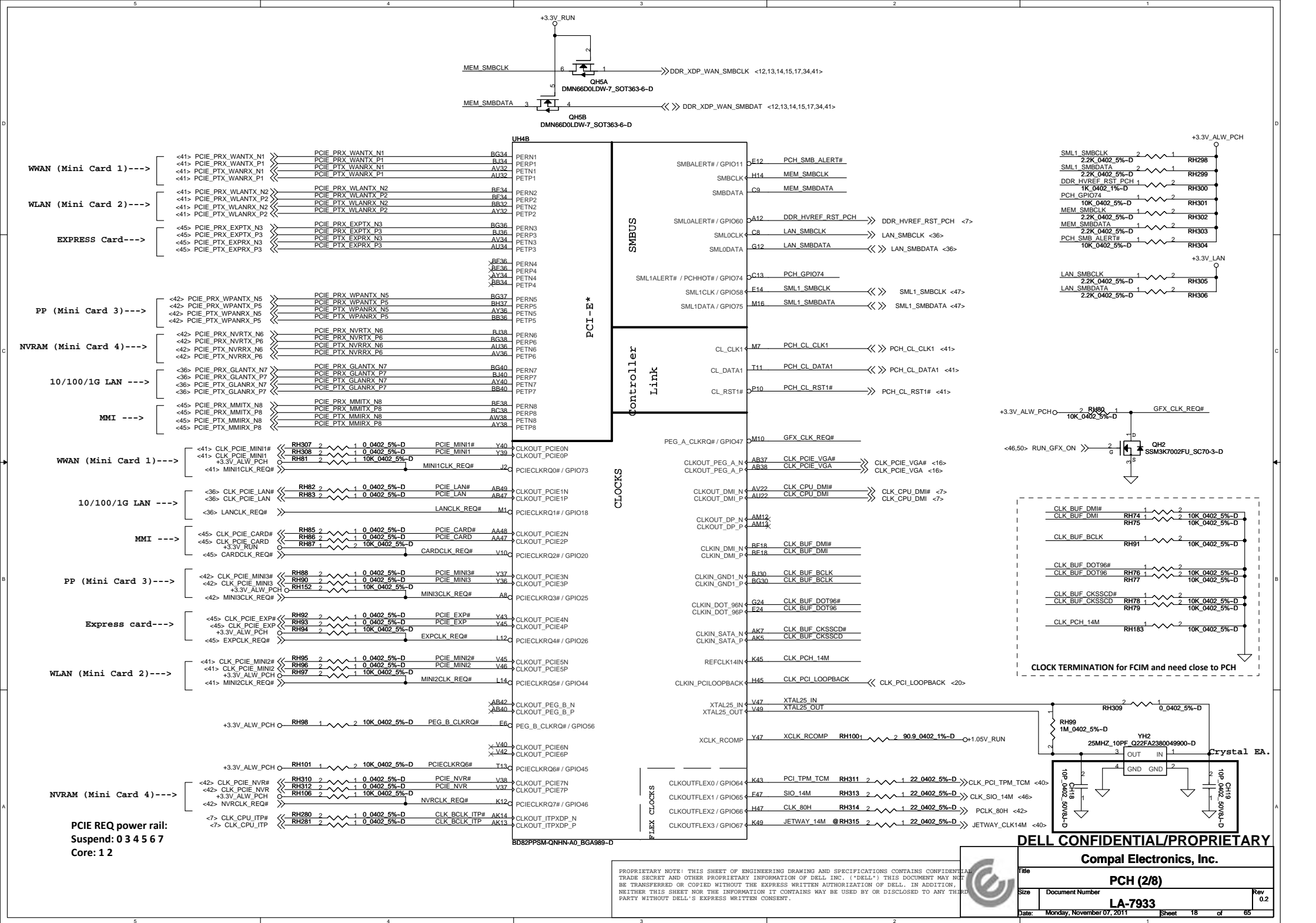
MXM

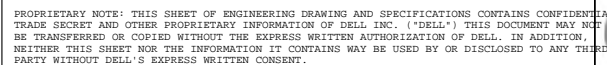
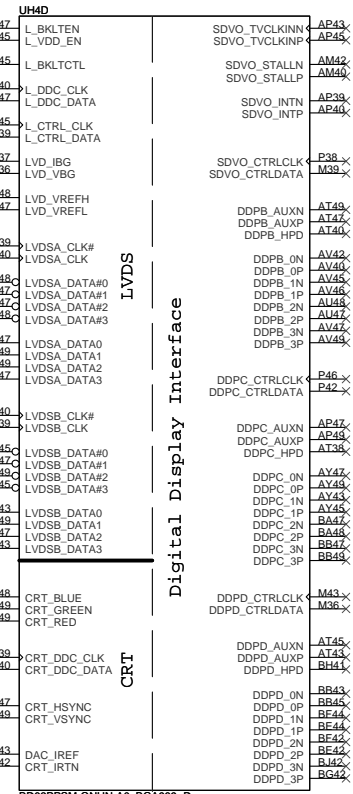
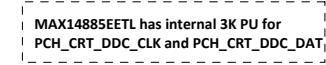
LA-7933

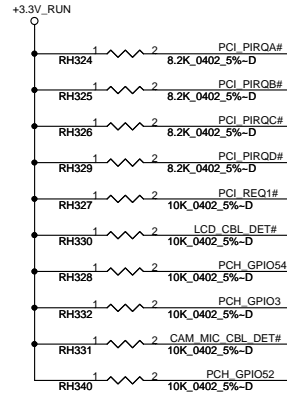
Date: Monday, November 07, 2011 Sheet 15 of 85

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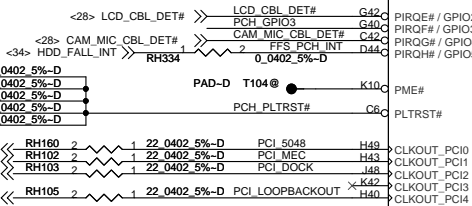
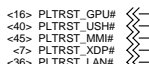




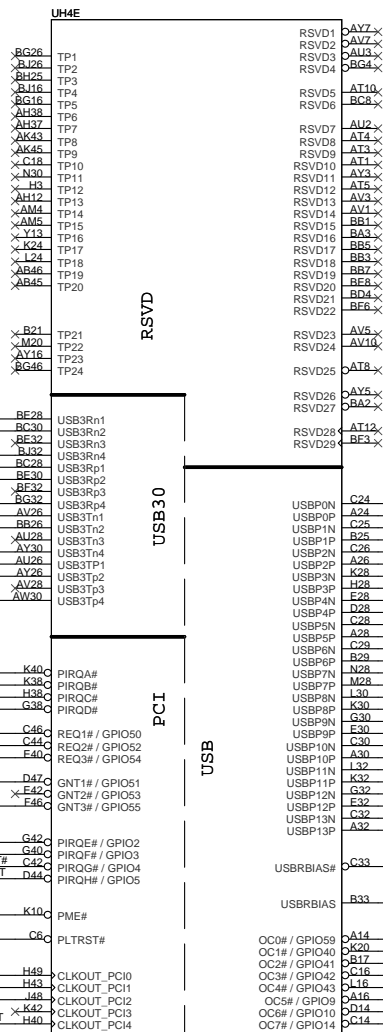
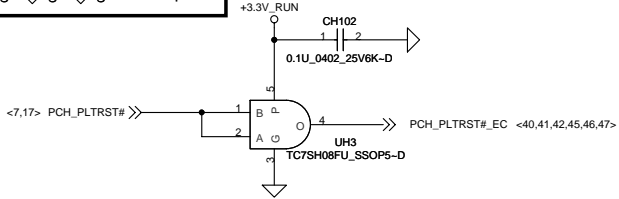
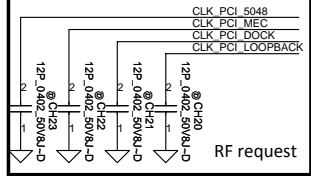




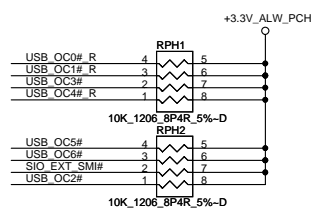
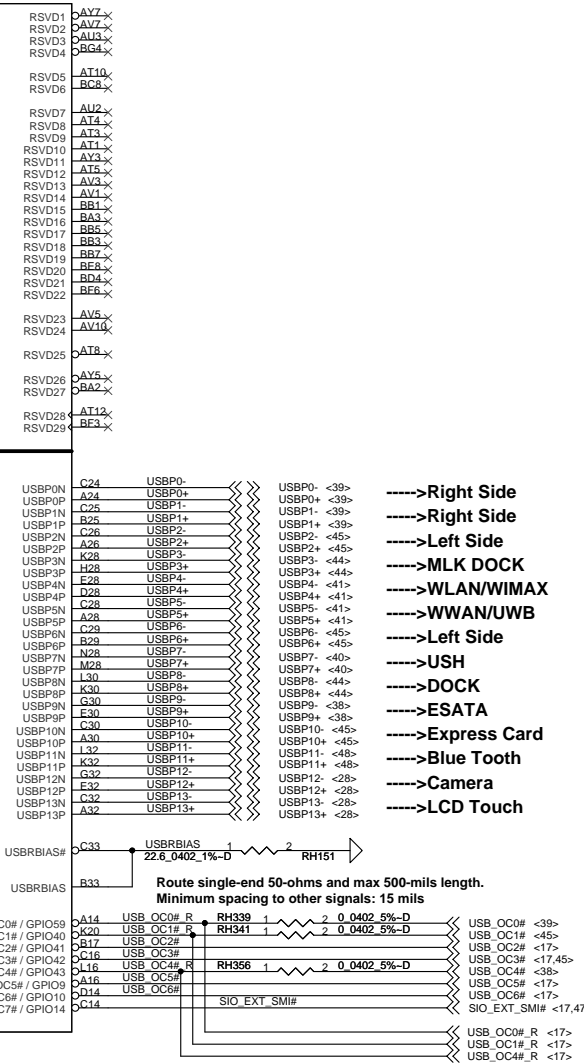
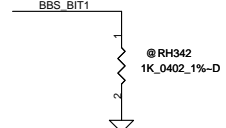
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



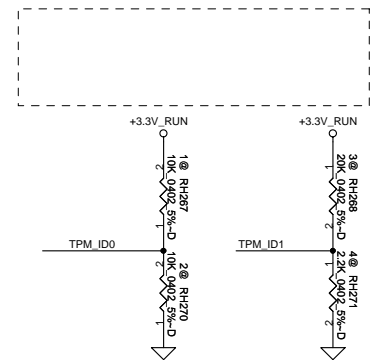
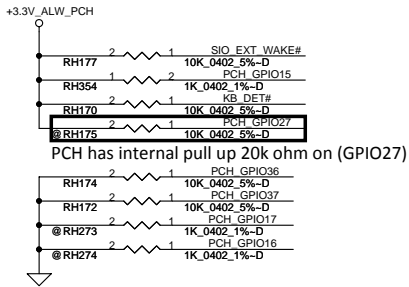
Avoid WWAN noise affect PCI 3,3M CLK.



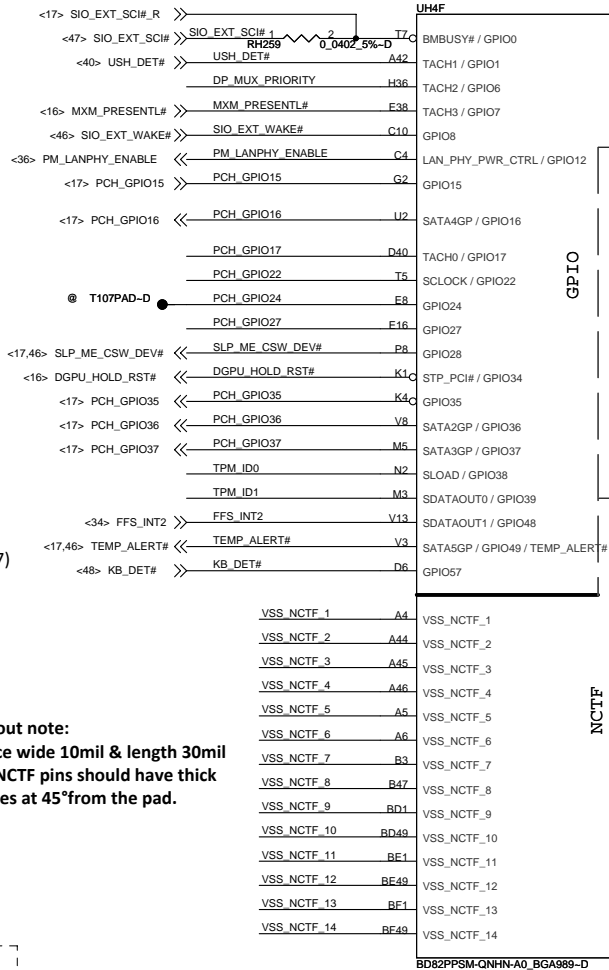
Boot BIOS Strap		
BBS_BIT1	SATA_SLDP (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE	
ENABLED	HIGH (DEFAULT)
DISABLED	LOW

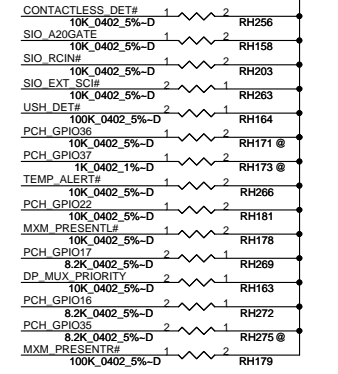


Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick
traces at 45° from the pad.

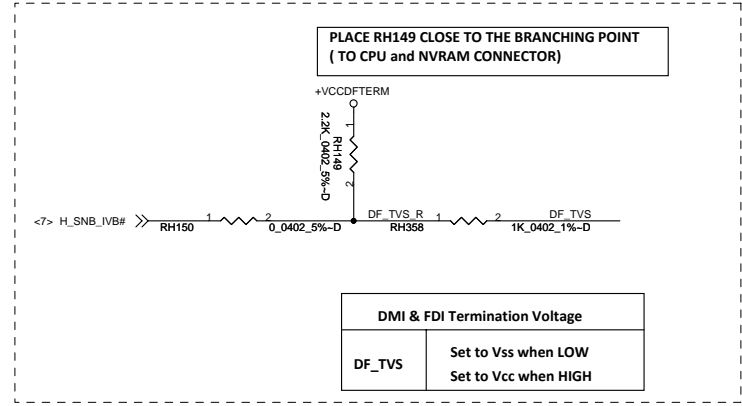


	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1

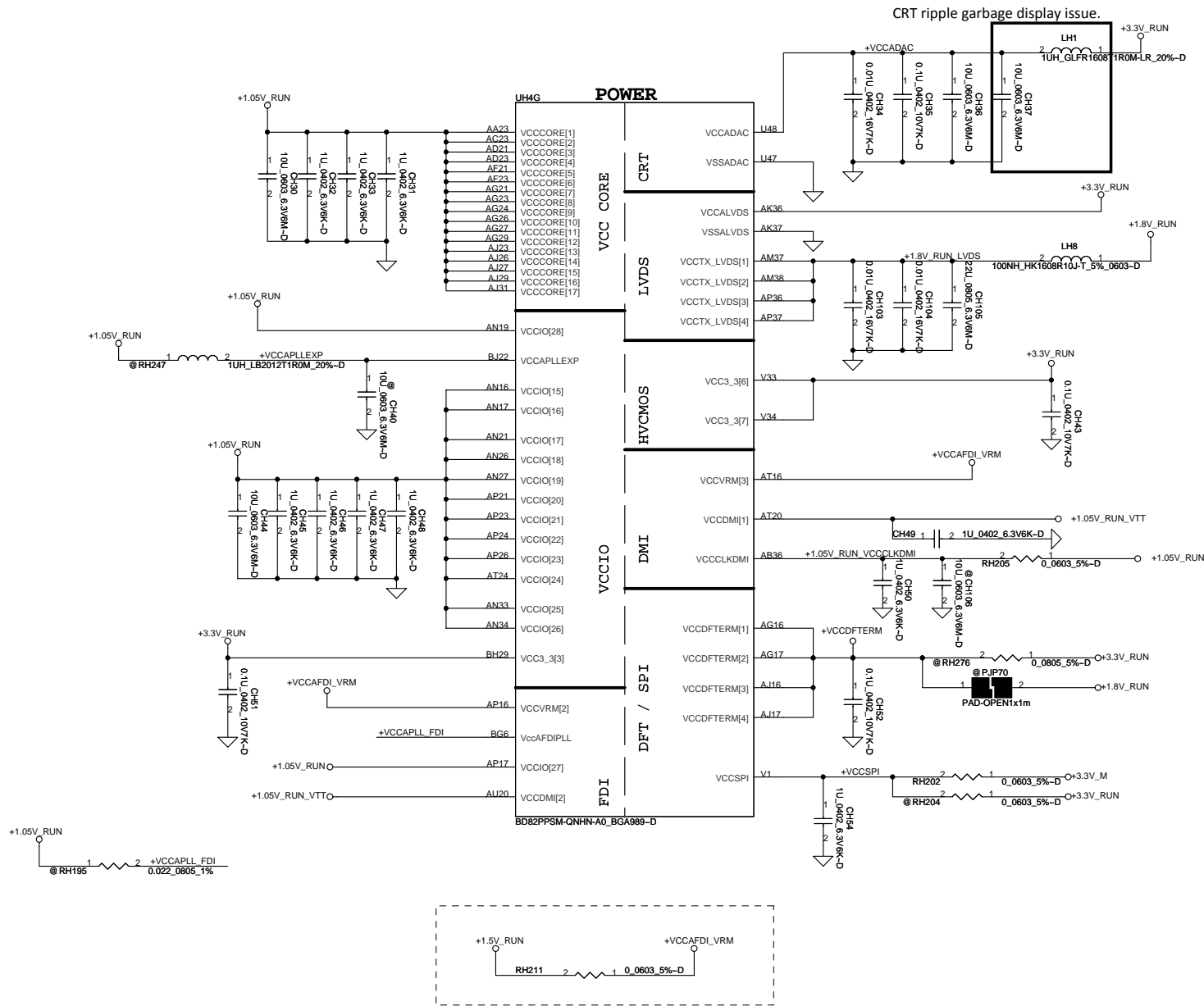
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Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick
traces at 45° from the pad.



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0.2



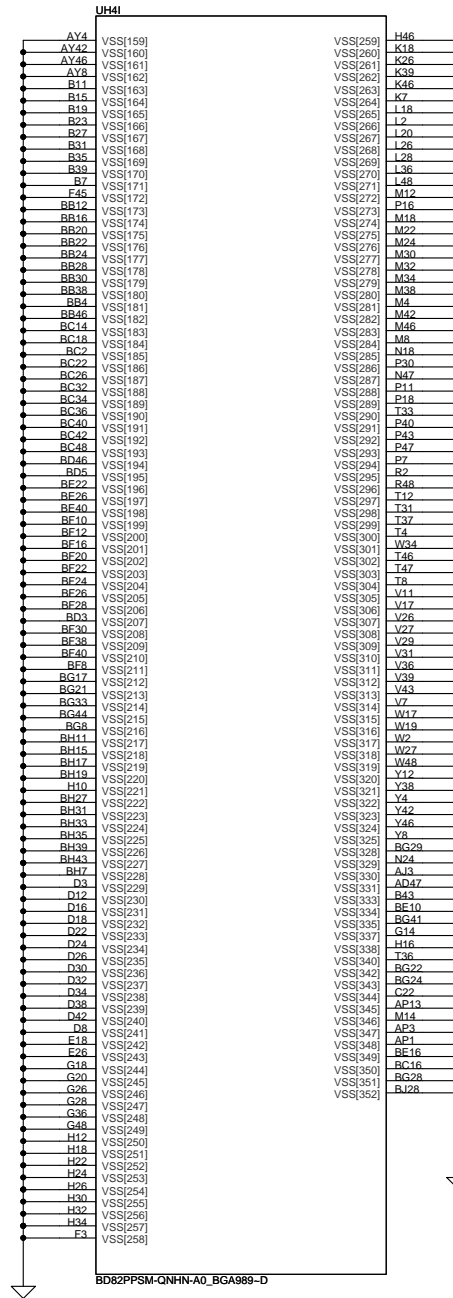
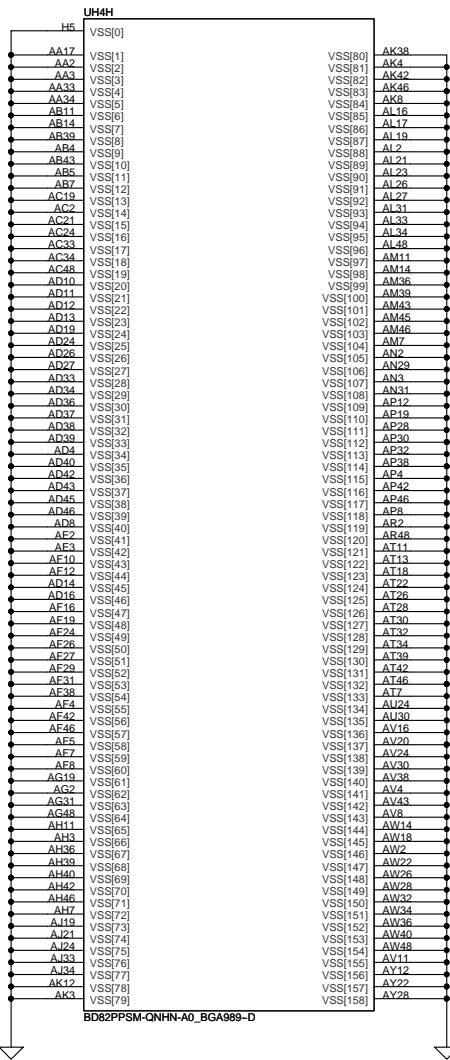
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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100k R10 200k R11 500V D1

Q17 2N2214A PNP

MMBT3904WT1G_SC70-3-D REM DIODE2_N_4002

100P 0.402 50V/8-A

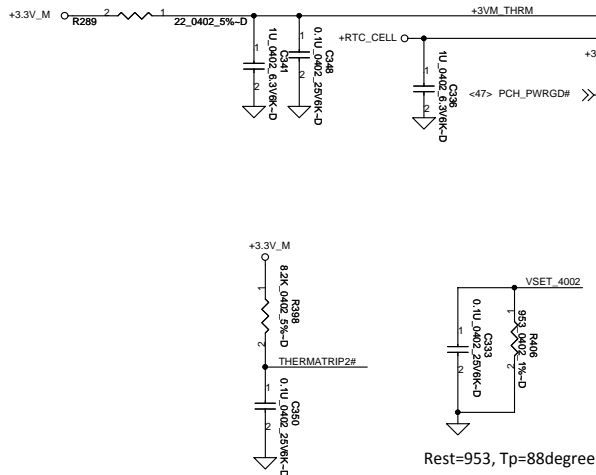
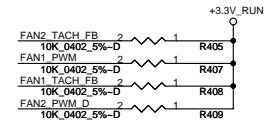
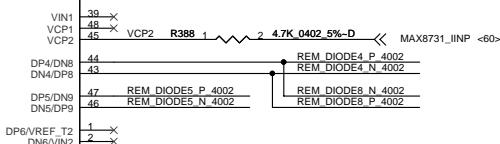
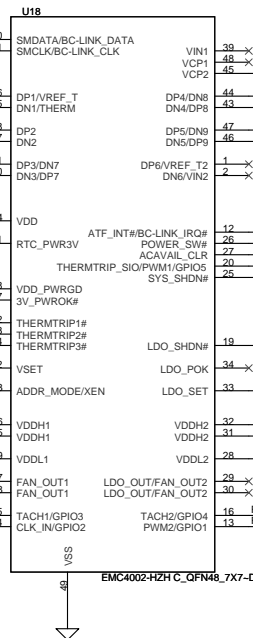
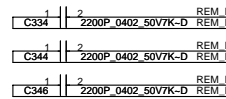
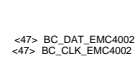
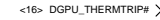
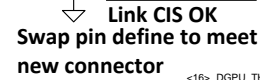
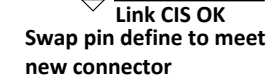
230V

REM DIODE3 P 4002

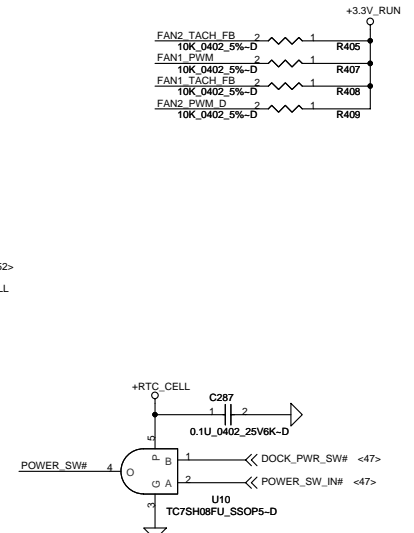
REM DIODE3 N 4002

Q14
MMBT3904WT1G SC70-3-D

C-79, 0.05 250V-0-250V 50/60Hz
 Q15
 MMBT3904WT1G SC70-3-D
 C335 close to U18
 2200µF 50V
 REM DIODE 4_N_4002

[illegible]

Rest=953, Tp=88degree



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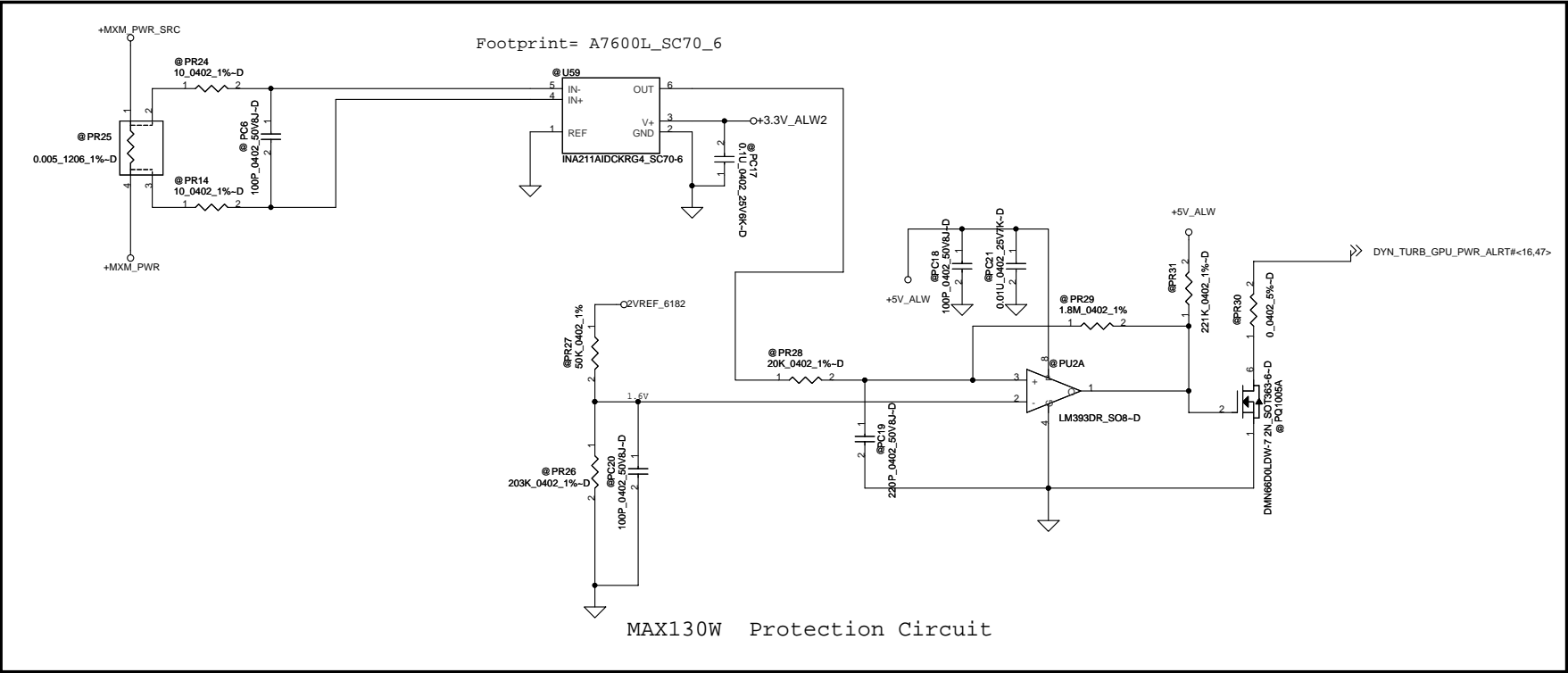
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Monitor PWR_SRC_MXM

RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)
100	1001_101(r/w)
180	1001_110(r/w)
300	1001_111(r/w)
430	1001_000(r/w)
560	1001_001(r/w)
750	1001_010(r/w)
1270	1001_011(r/w)
1600	0101_000(r/w)
2000	0101_001(r/w)
2700	0101_010(r/w)
3600	0101_011(r/w)
5600	0101_100(r/w)
9100	0101_100(r/w)
20000	0101_101(r/w)
Open	0011_000(r/w)

Monitor PWR_SRC_MXM for DELL request



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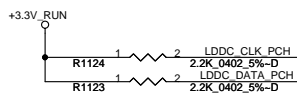
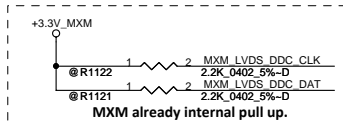
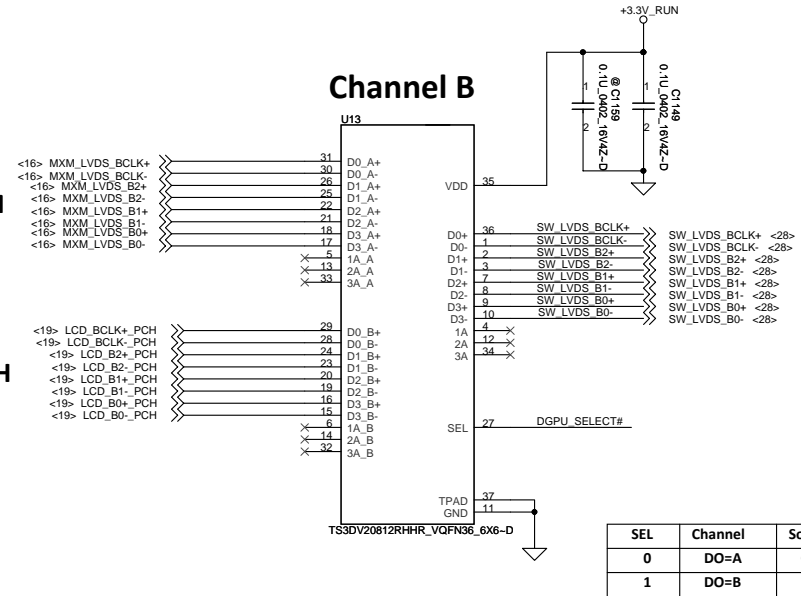
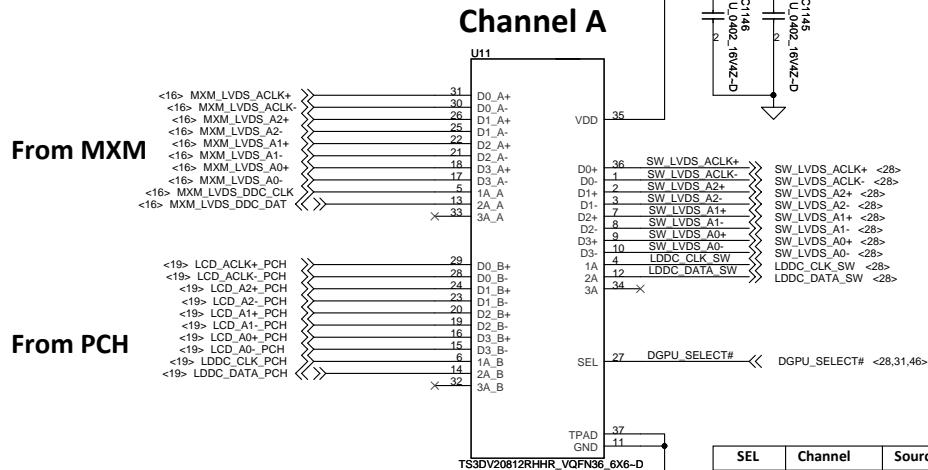
Current Sensor

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LVDS SW

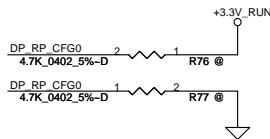
LA-7933

Rev 0.2

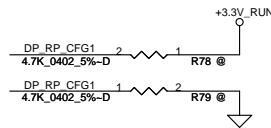
Date: Monday, November 07, 2011

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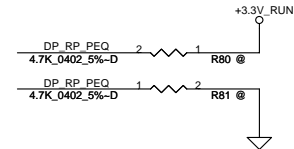
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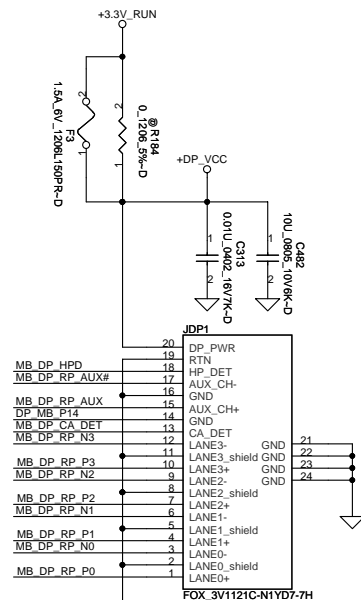
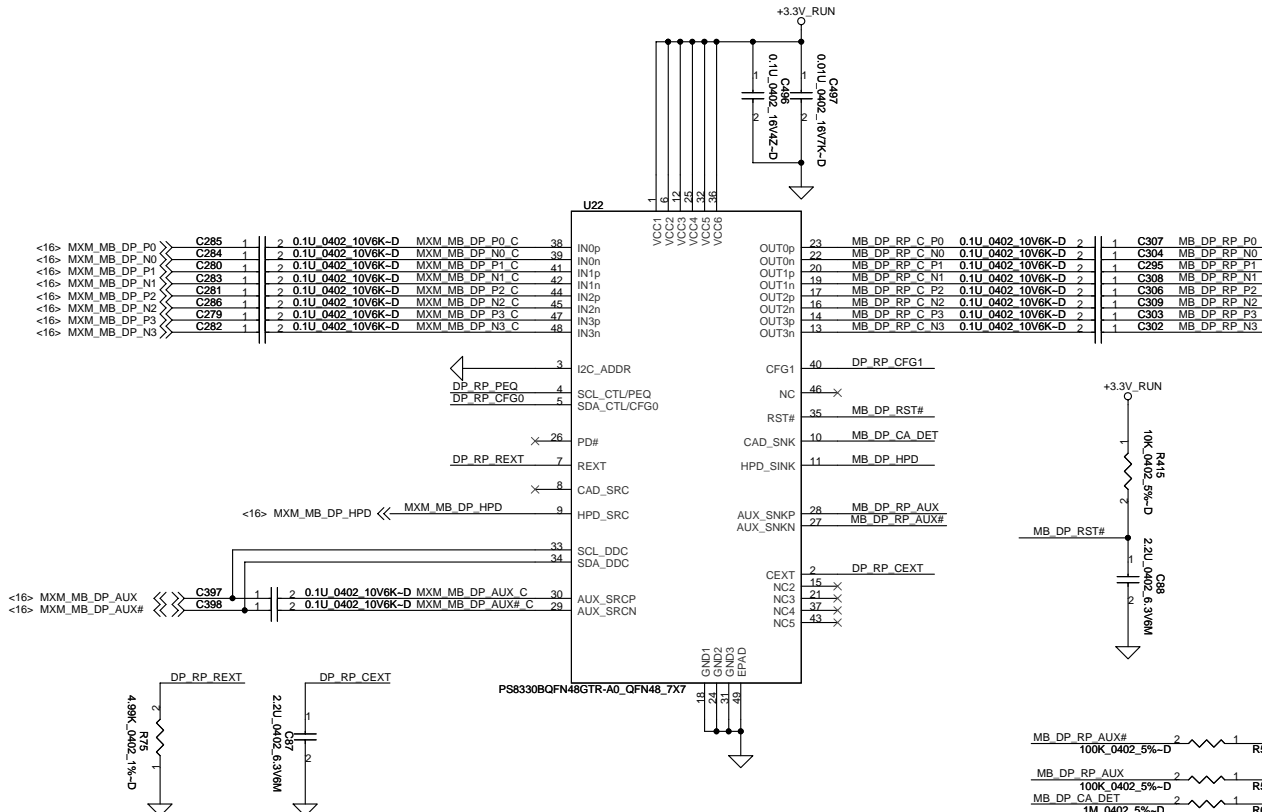
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
 L: default, automatic EQ enable & AUX interception enable
 H: automatic EQ disable & AUX interception enable
 M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing



Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
 H: default, auto test disable & input offset cancellation enable
 L: auto test enable & input offset cancellation enable
 M: auto test disable & input offset cancellation disable



Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2
 H: HEQ, compensate channel loss up to 15dB @ HBR2
 M: LLEQ, compensate channel loss up to 5dB @ HBR2

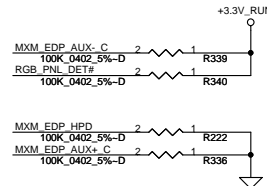
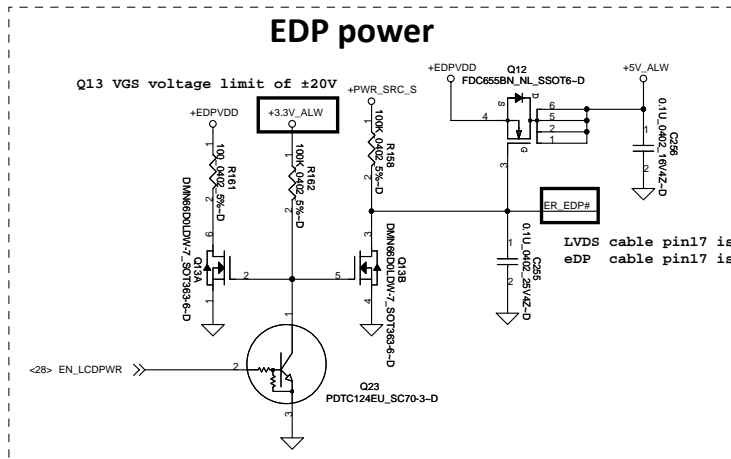


Link CIS
 Vendor change MPN to 3V11211-NBYD7-7H
 but no modif PCB footprint

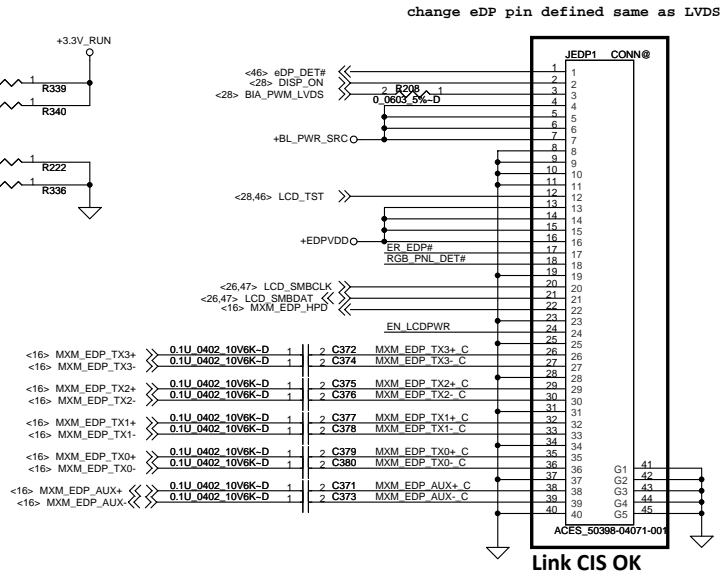
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		DP CONN	
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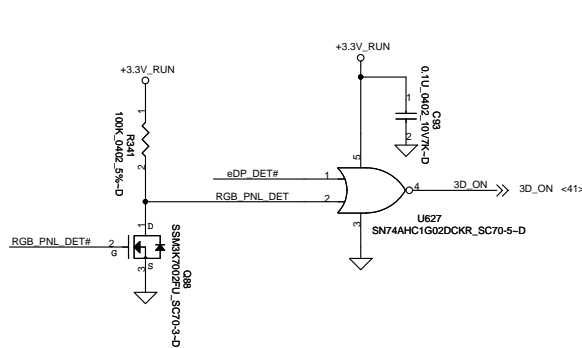
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LVDS cable pin17 is GND and
EDP cable pin17 is floating(ER_EDP#)

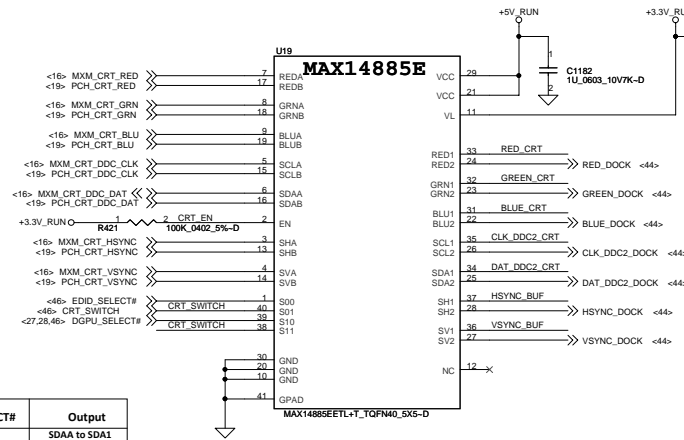


Link CIS OK



Channel A --> GPU

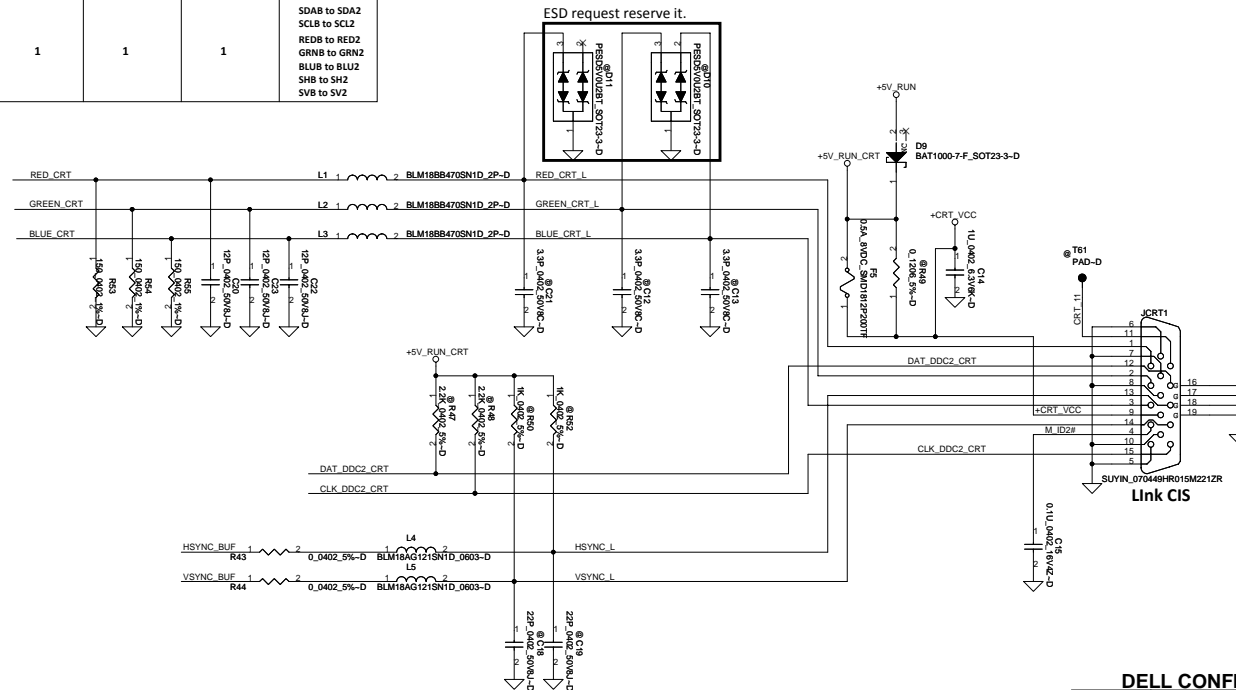
Channel B --> PCH



Port 1 --> MB board CRT

Port 2 --> Docking Port RGB

	CRT_SWITCH	DGPU_SELECT#	EDID_SELECT#	Output
DSC mode output to MB VGA	0	0	0	SDAA to SDA1 SCLA to SCL1 REDA to RED1 GRNA to GRN1 BLUA to BLU1 SHA to SH1 SVA to SV1
DSC mode output to docking VGA	1	0	0	SDAA to SDA2 SCLA to SCL2 REDA to RED2 GRNA to GRN2 BLUA to BLU2 SHA to SH2 SVA to SV2
UMA mode output to MB VGA	0	1	1	SDAB to SDA1 SCLB to SCL1 REDB to RED1 GRNB to GRN1 BLUB to BLU1 SHB to SH1 SVB to SV1
UMA mode output to docking VGA	1	1	1	SDAB to SDA2 SCLB to SCL2 REDB to RED2 GRNB to GRN2 BLUB to BLU2 SHB to SH2 SVB to SV2

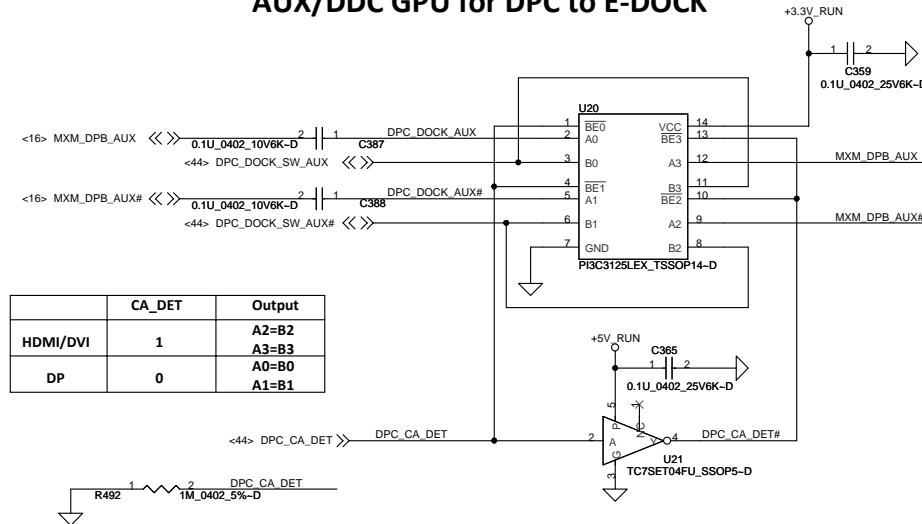


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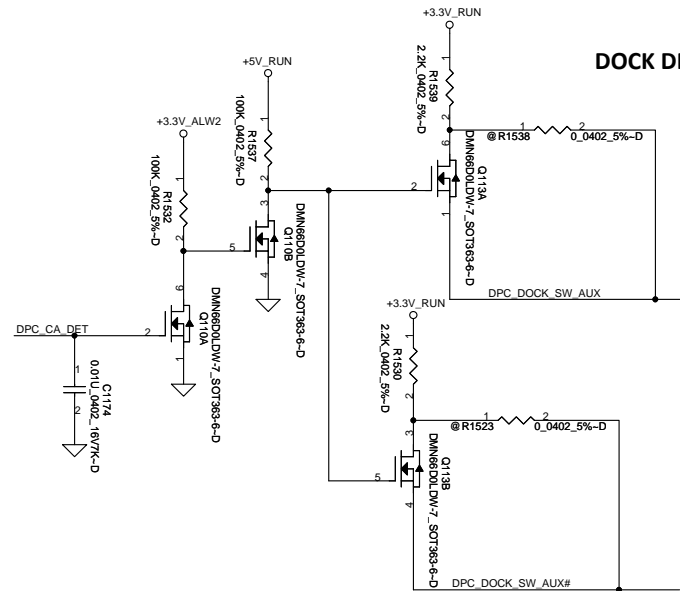
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File	VGA CONN	Rev	0.2
Size	Document Number	LA-7933	
Date	Tuesday, November 08, 2011	Sheet	31 of 65

AUX/DDC GPU for DPC to E-DOCK



DOCK DPB(PORT2) DDC

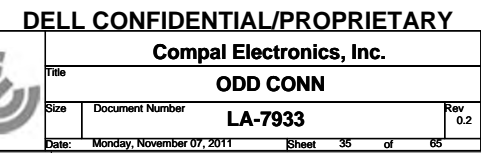


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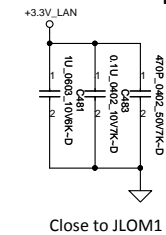
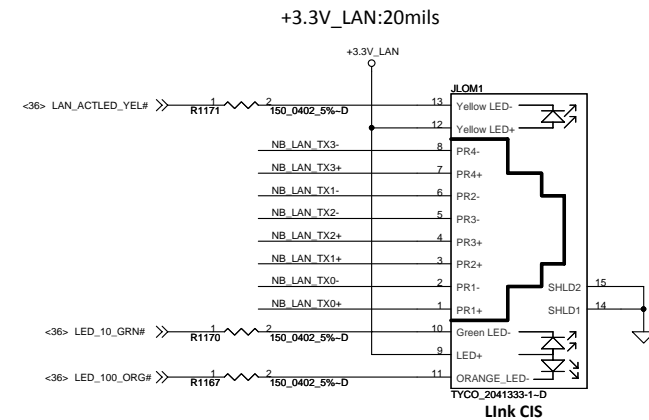
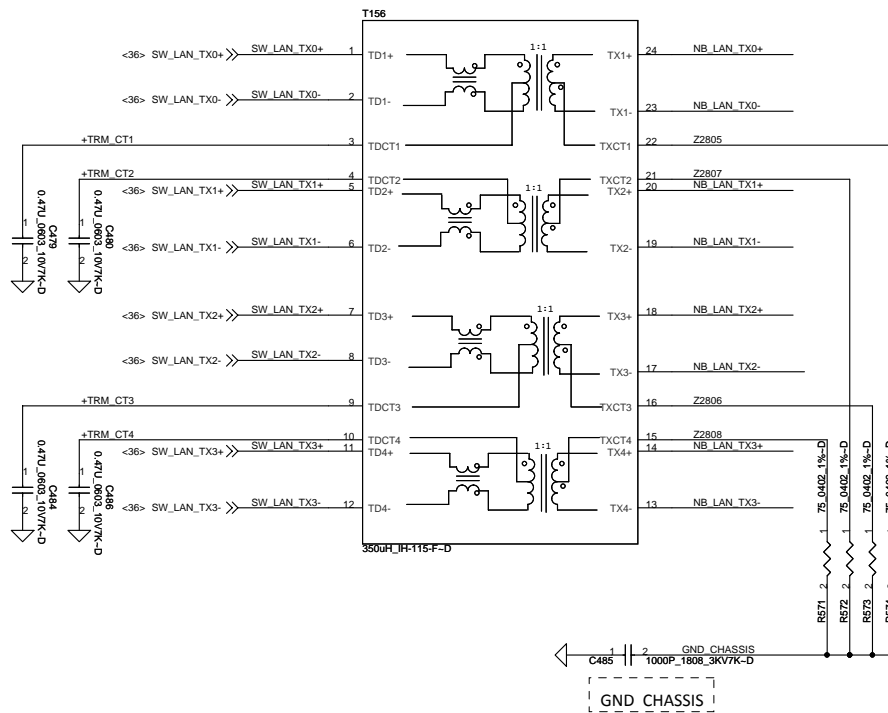
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Title			
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Size	Document Number		Rev
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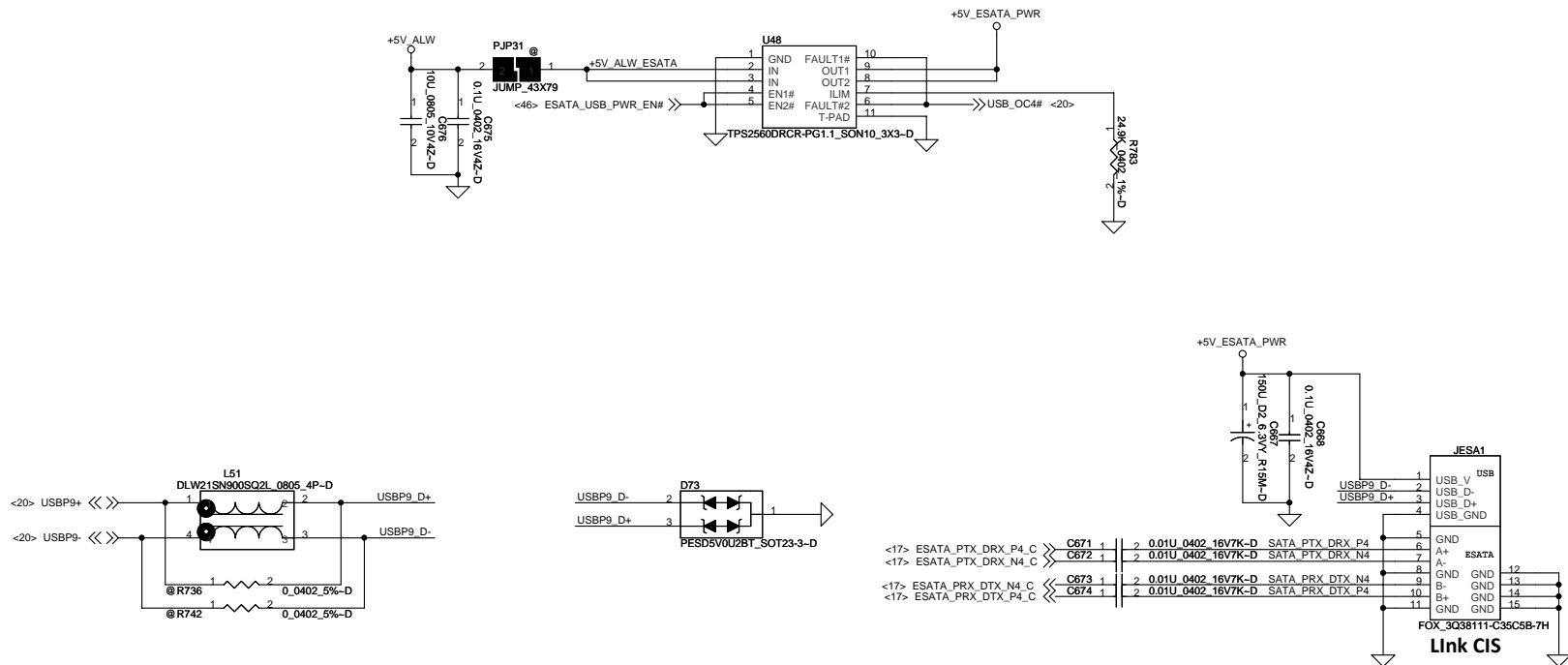


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Size		Document Number	
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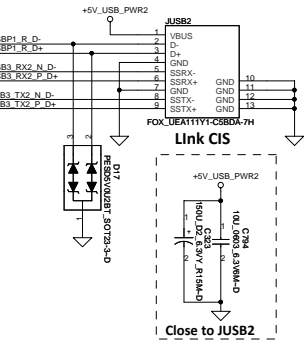
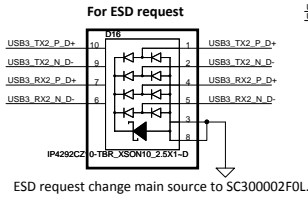
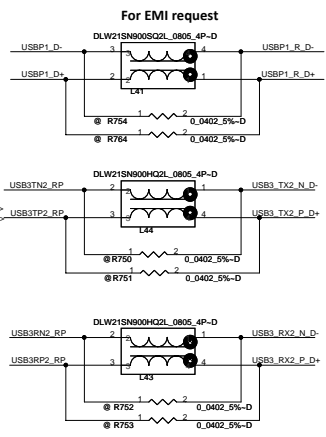
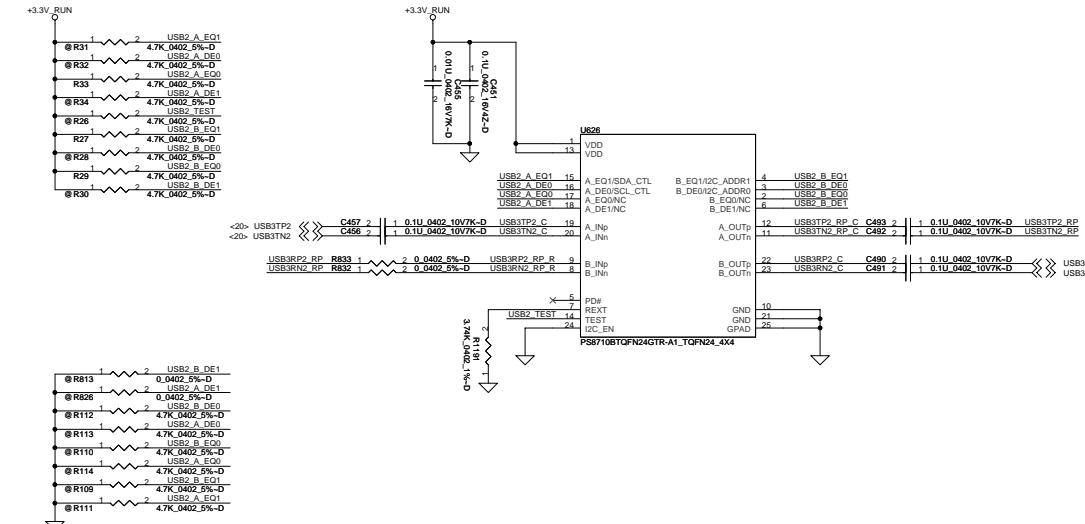
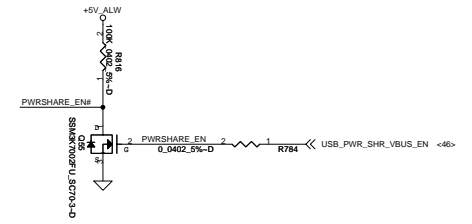
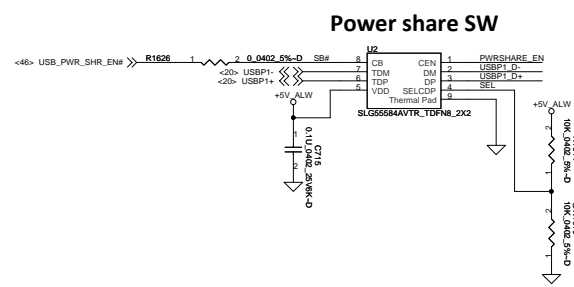
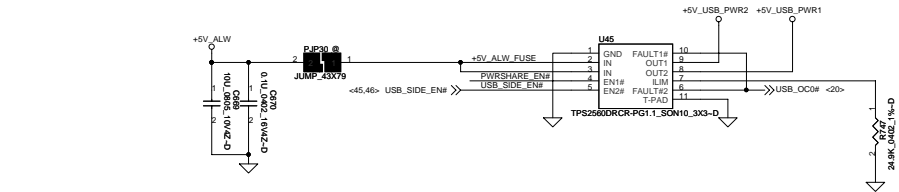
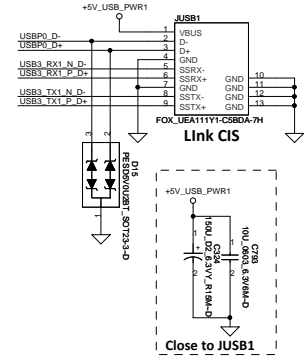
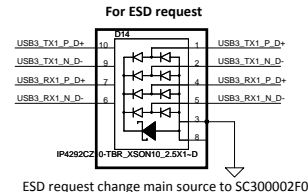
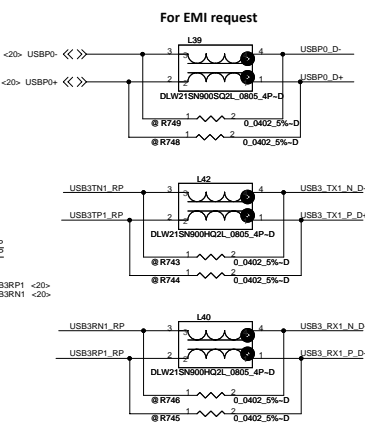
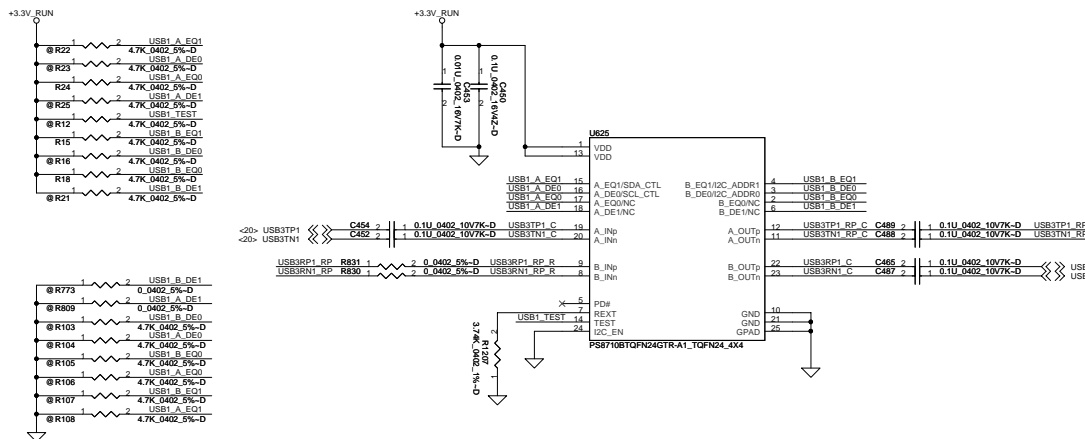
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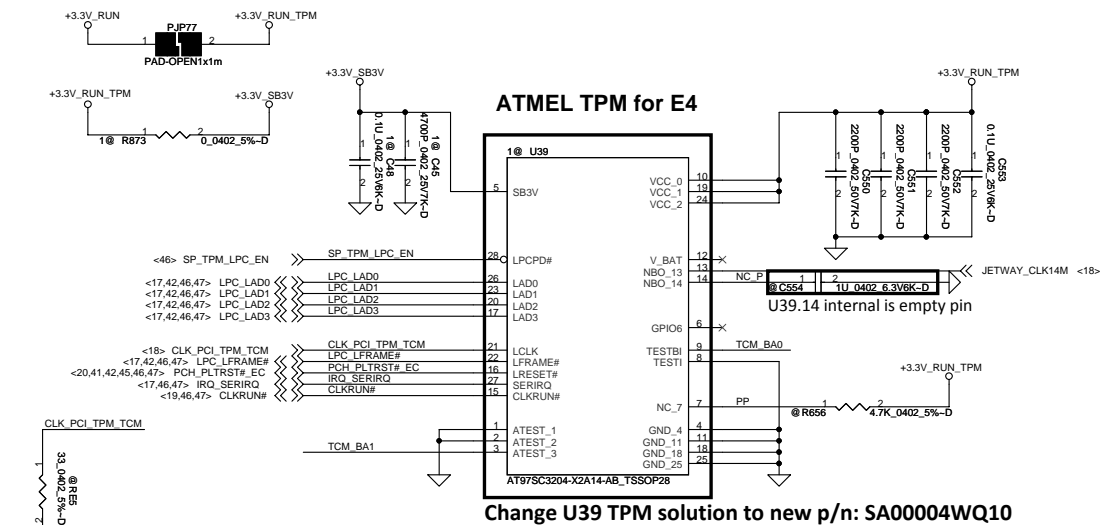
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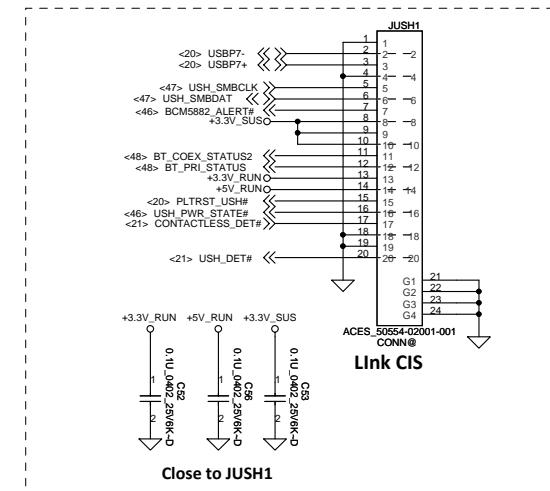
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Size	Document Number	LA-7933	Rev 0.2
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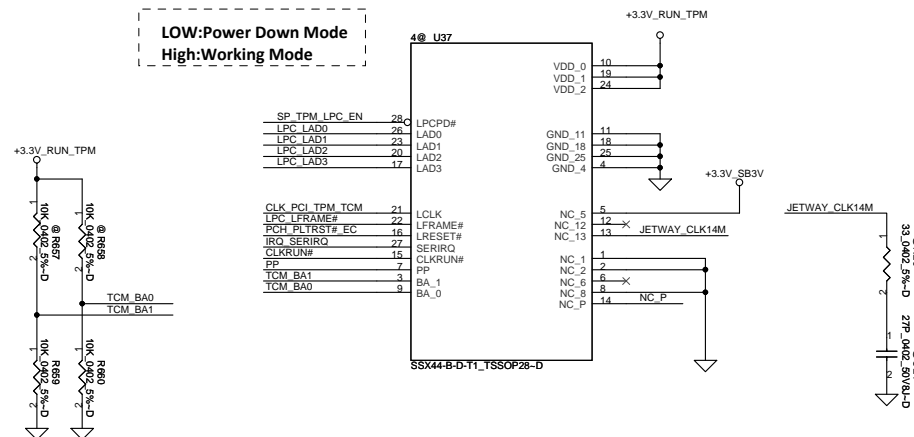


Co-lay U37 and U39

LPC layout: Place TCM first and then end LPC with TPM.



China TCM: NationZ & Jetway co-lay



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TPM/TCM

File
Size
Date: Monday, November 07, 2011

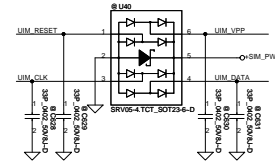
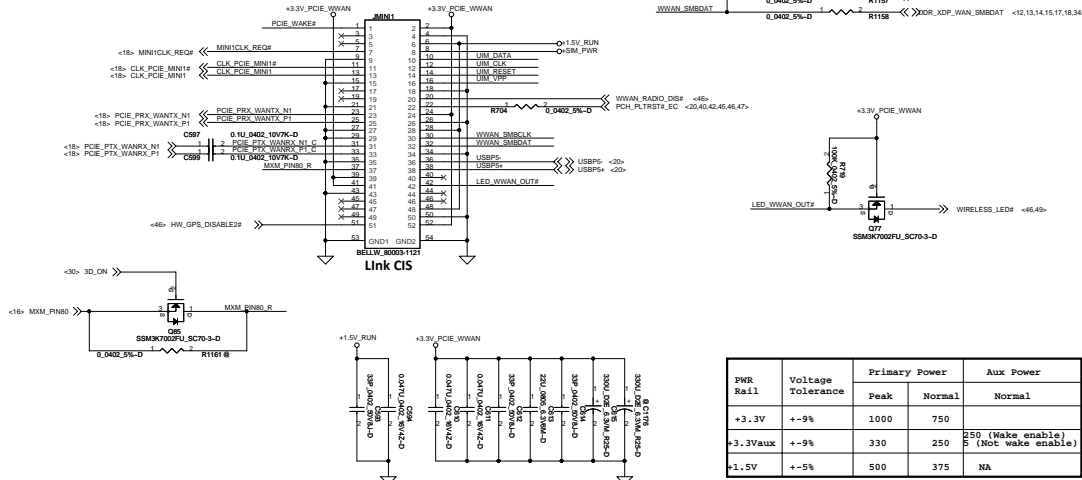
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Rev
0.2

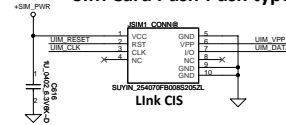
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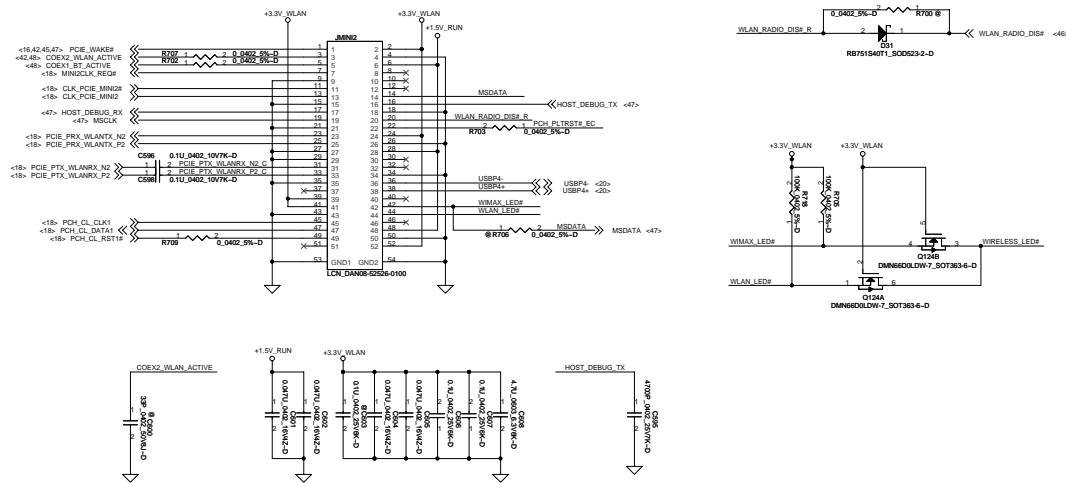
Mini WWAN/GPS/LTE H= 4 mm



SIM Card Push-Push type



Mini WLAN/WIMAX H=5.2



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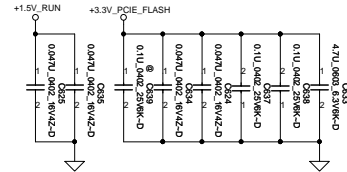
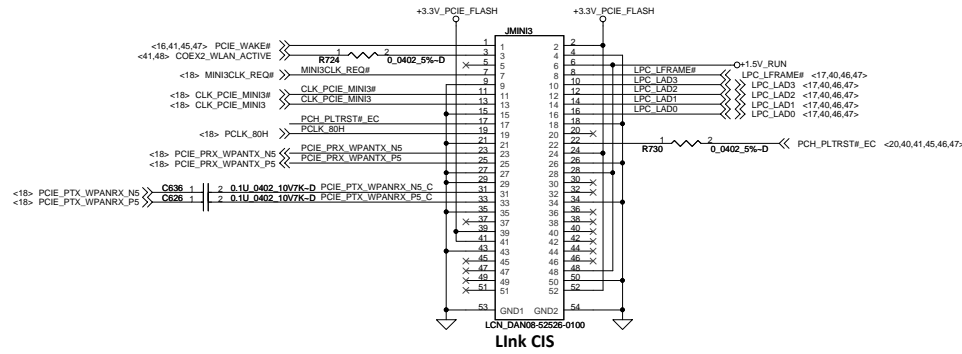
Mini Card-1/2

LA-7933

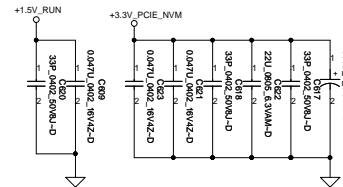
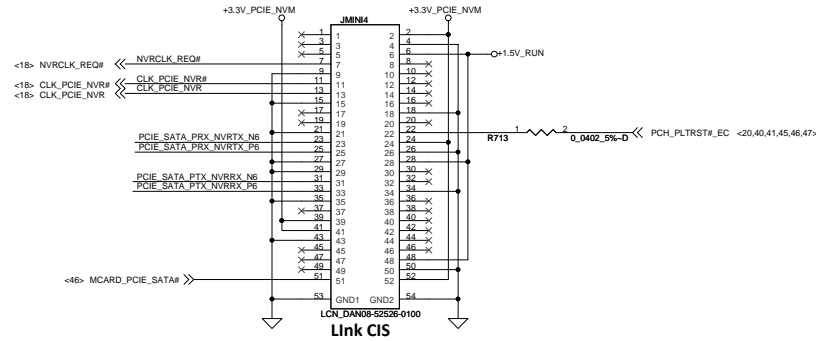
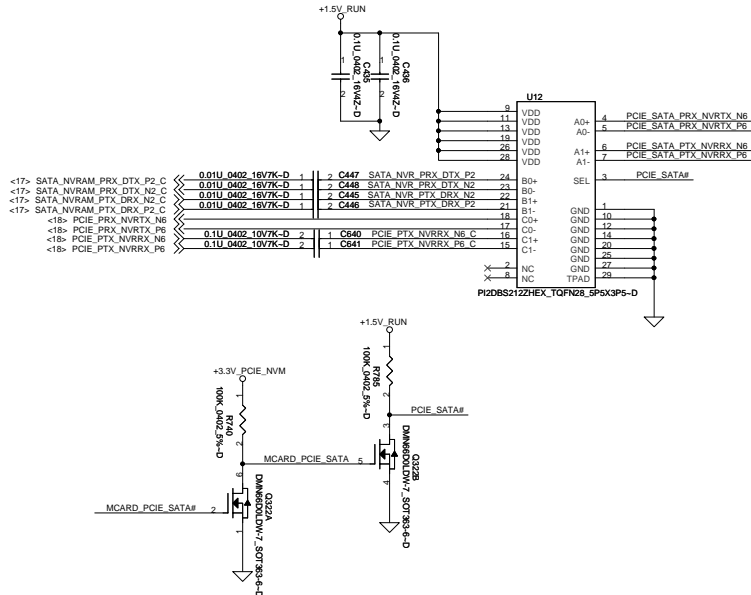
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Pink Pather H=5.2



NVRAM H=5.2



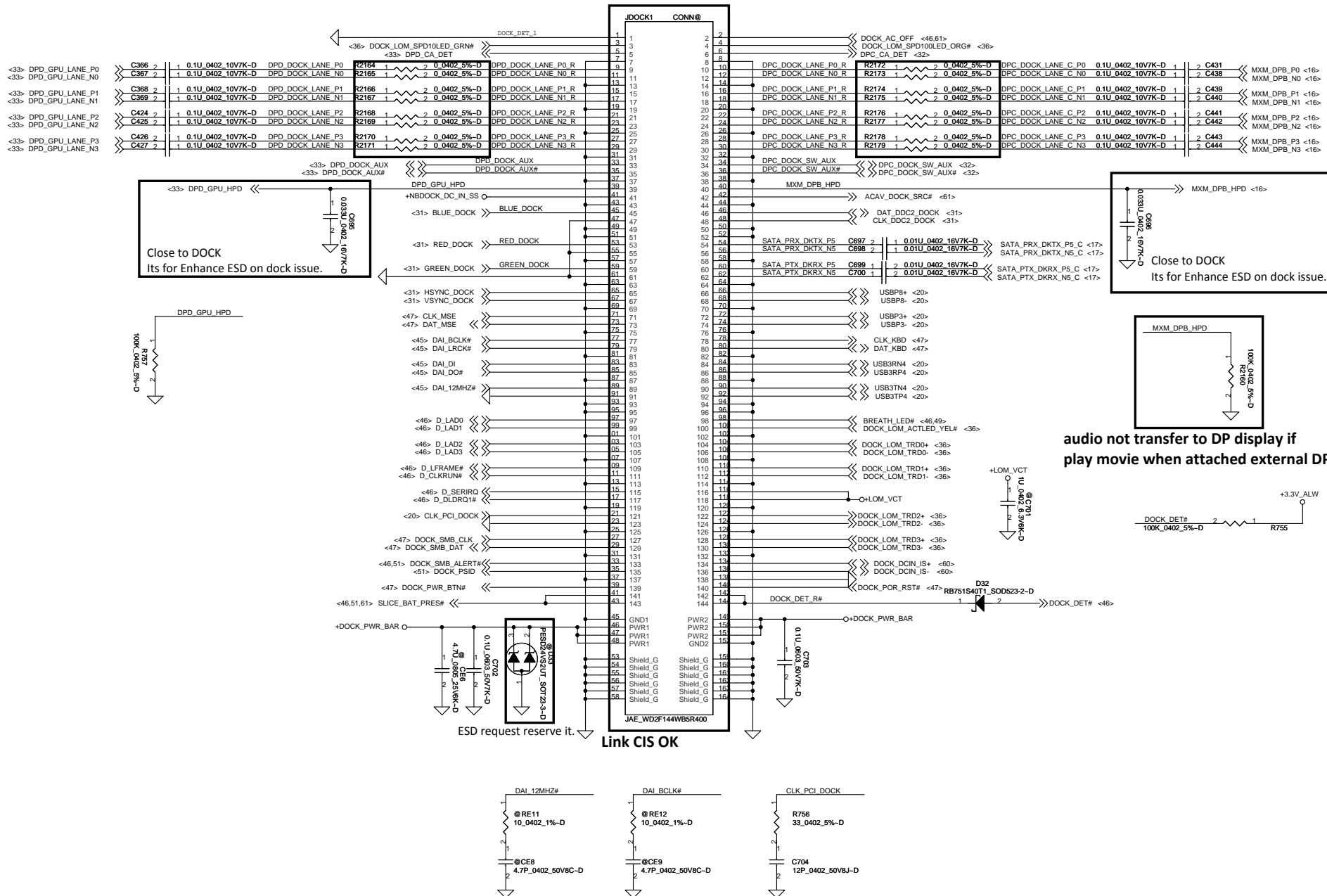
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EMI request add 33ohm for DOCK DVI signals.



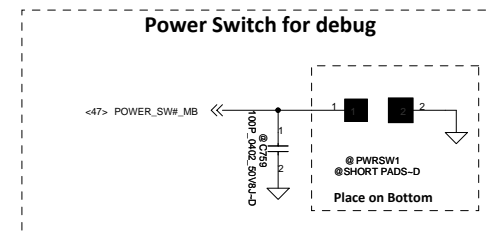
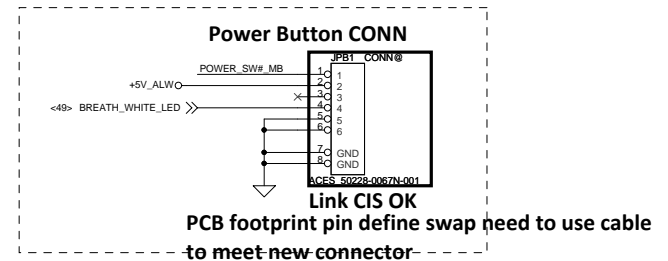
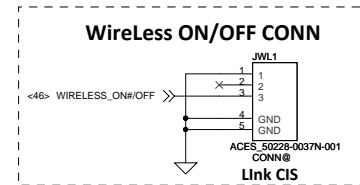
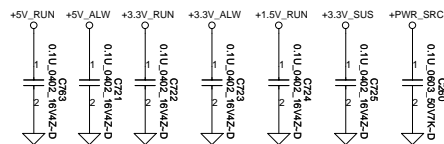
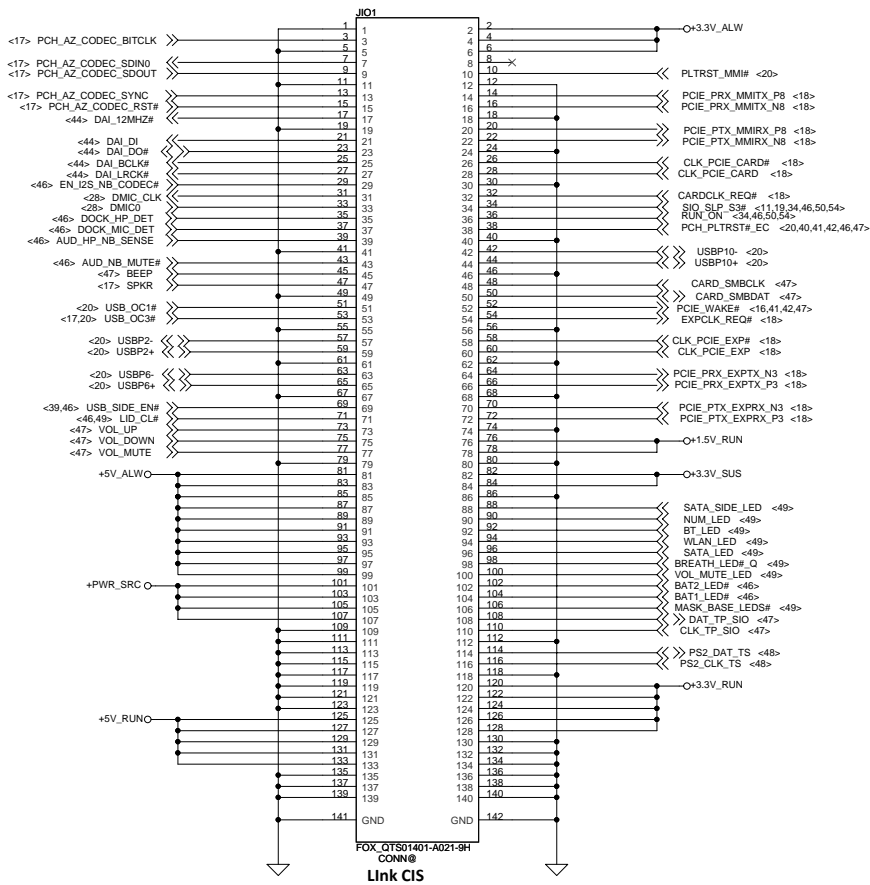
**audio not transfer to DP display if
play movie when attached external DP display**

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Title			
Docking			
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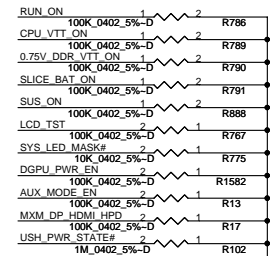
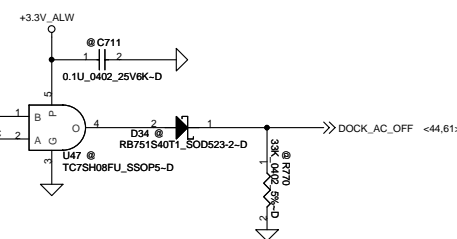
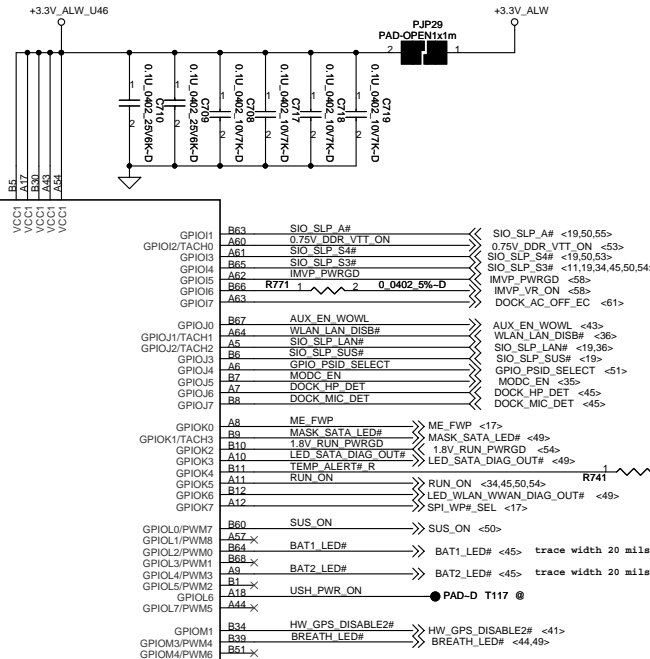
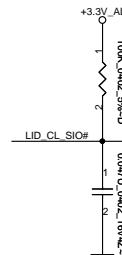
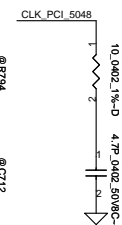
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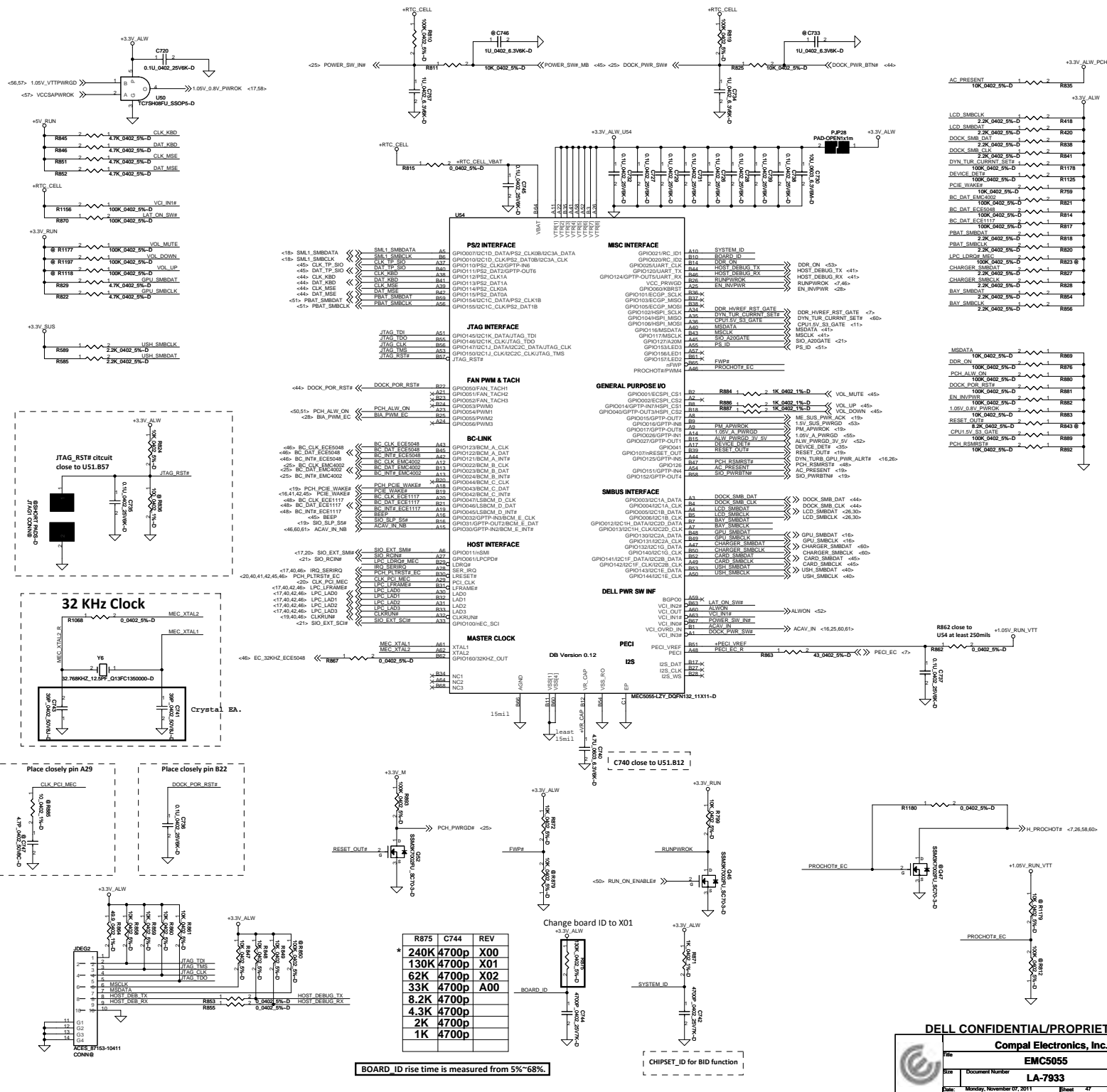
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	VGA_ID0
Discrete	0
UMA	1

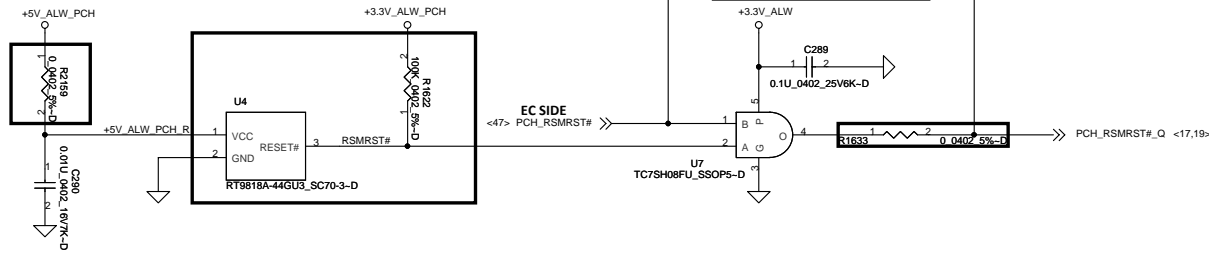


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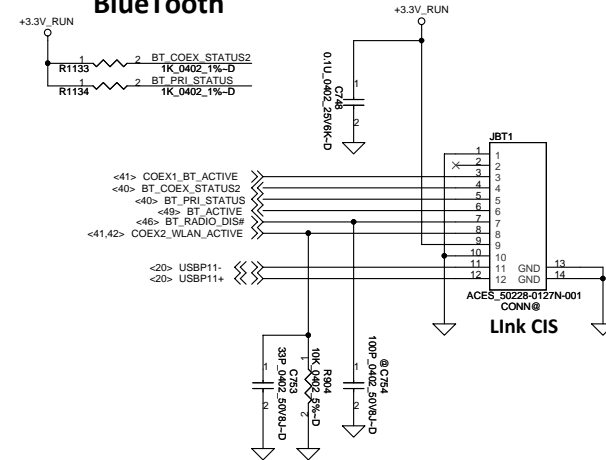


RSMRST circuit

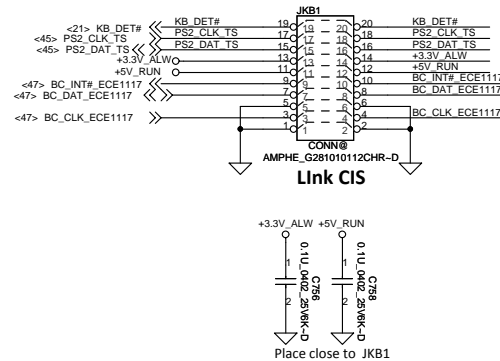
For meet T235(power off)= min 40ns(SPEC).T08a(power on)= max 90ms.



BlueTooth



Keyboard



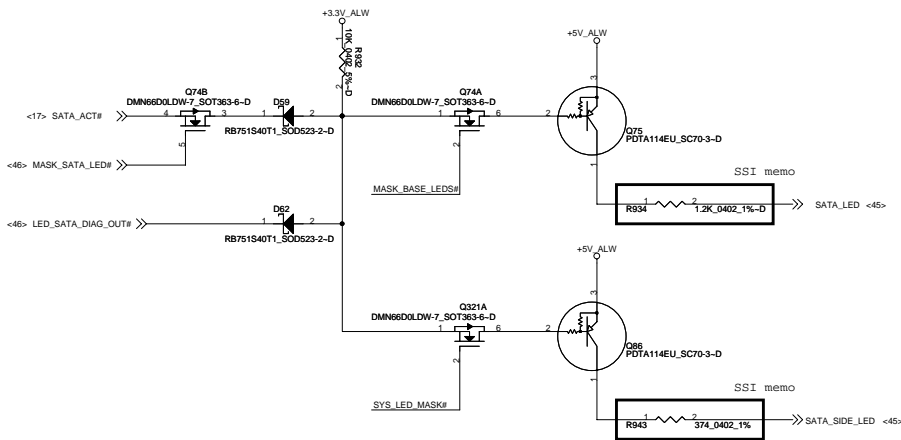
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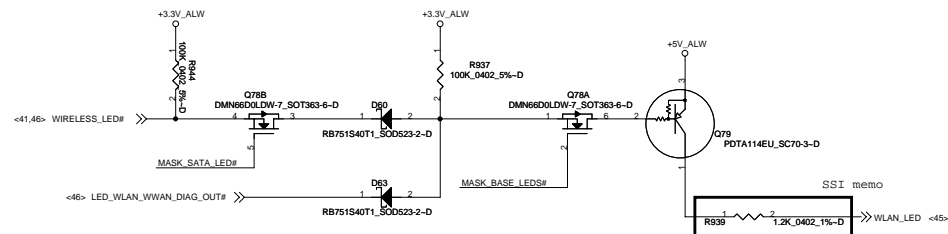
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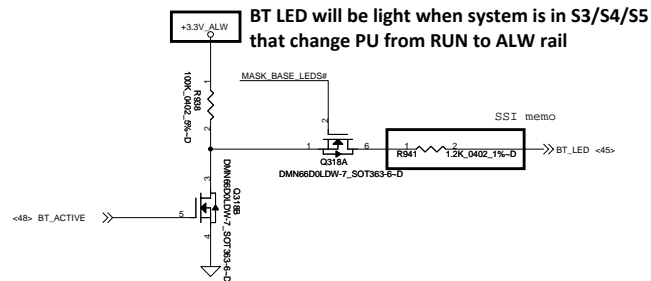
HDD LED



WWAN/WLAN LED

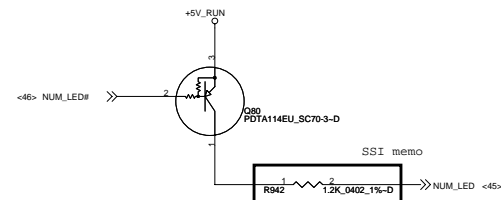


BT LED

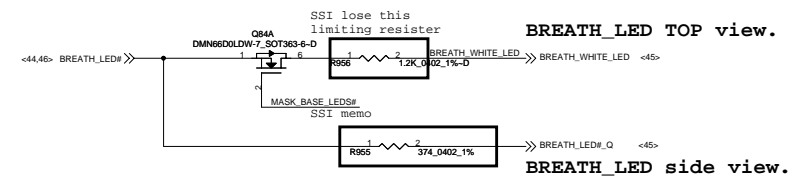


BT LED will be light when system is in S3/S4/S5 that change PU from RUN to ALW rail

NUM LED



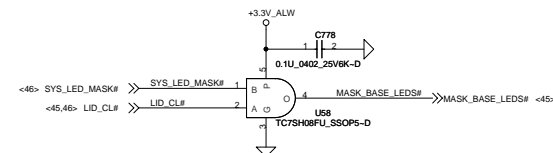
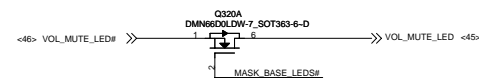
Breath LED



BREATH_LED TOP view.

BREATH_LED side view.

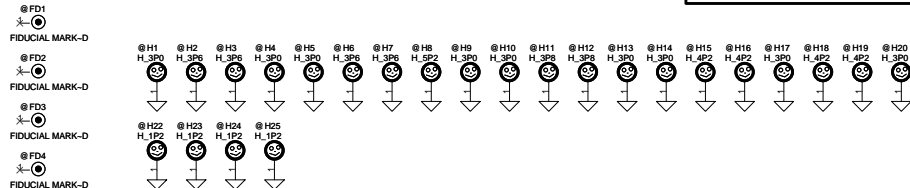
Volume mute LED



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark



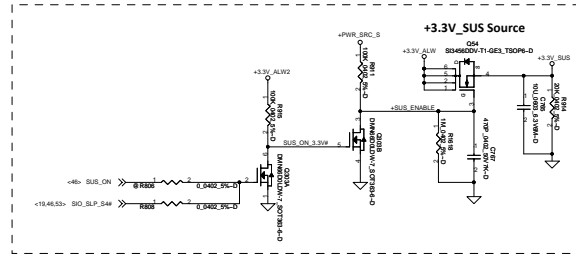
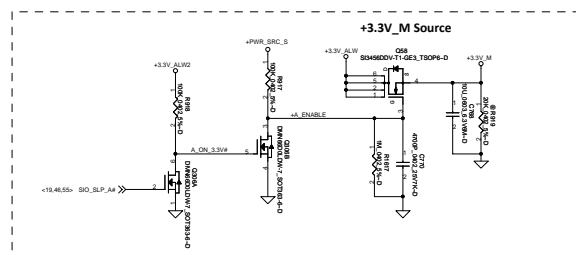
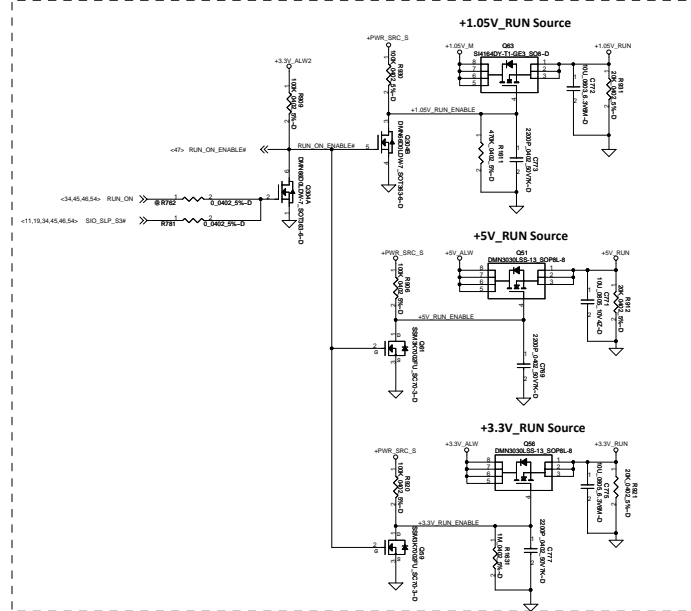
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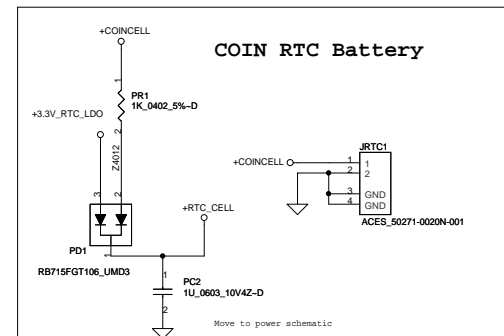
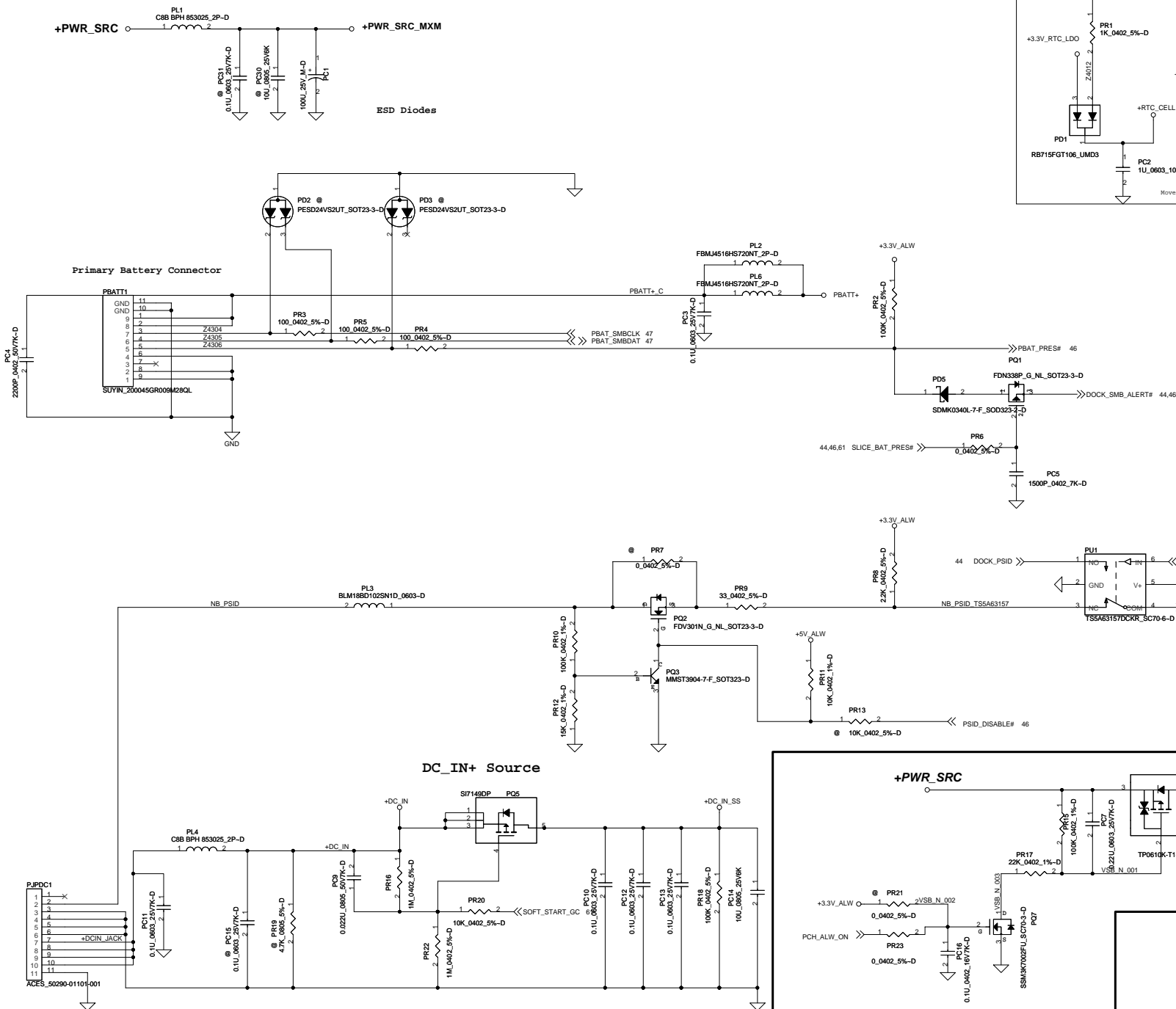
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PAD & Standoff & LED

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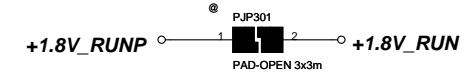
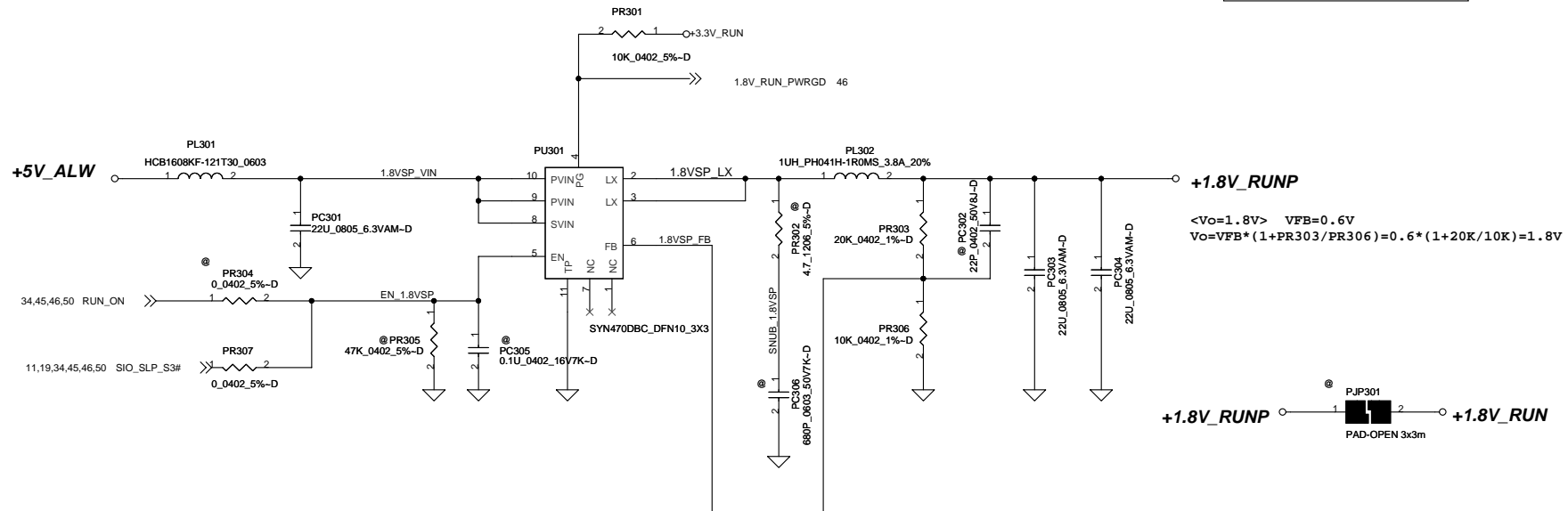


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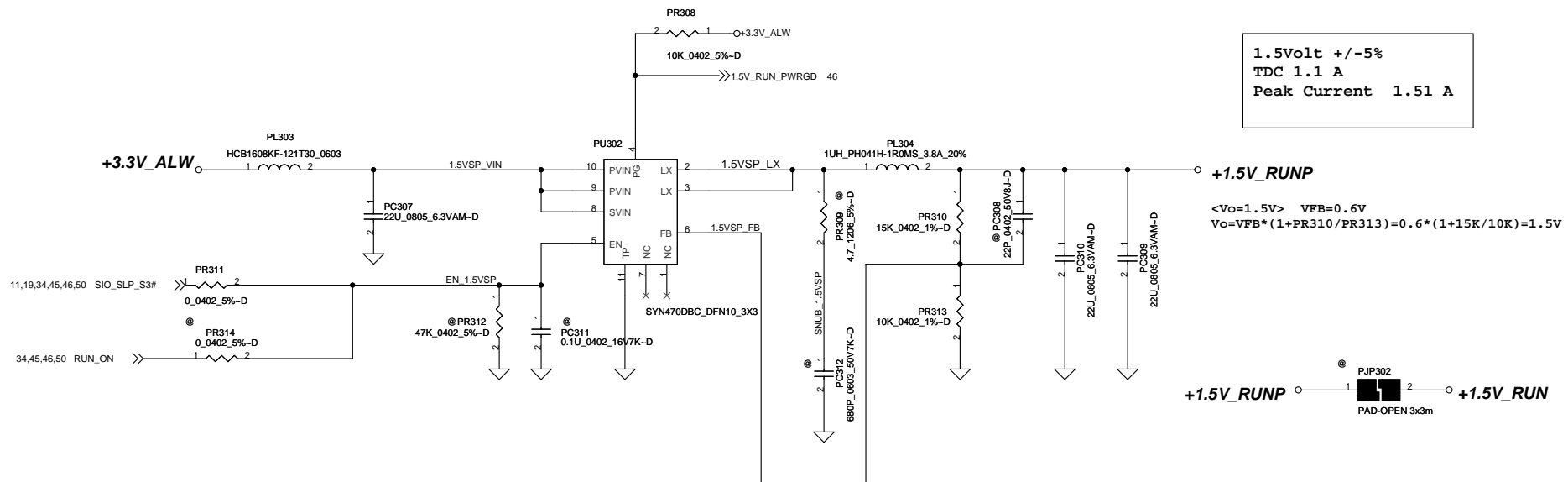
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1.8Volt +/-5%
TDC 0.65A
Peak Current 0.93A



1.5Volt +/-5%
TDC 1.1 A
Peak Current 1.51 A

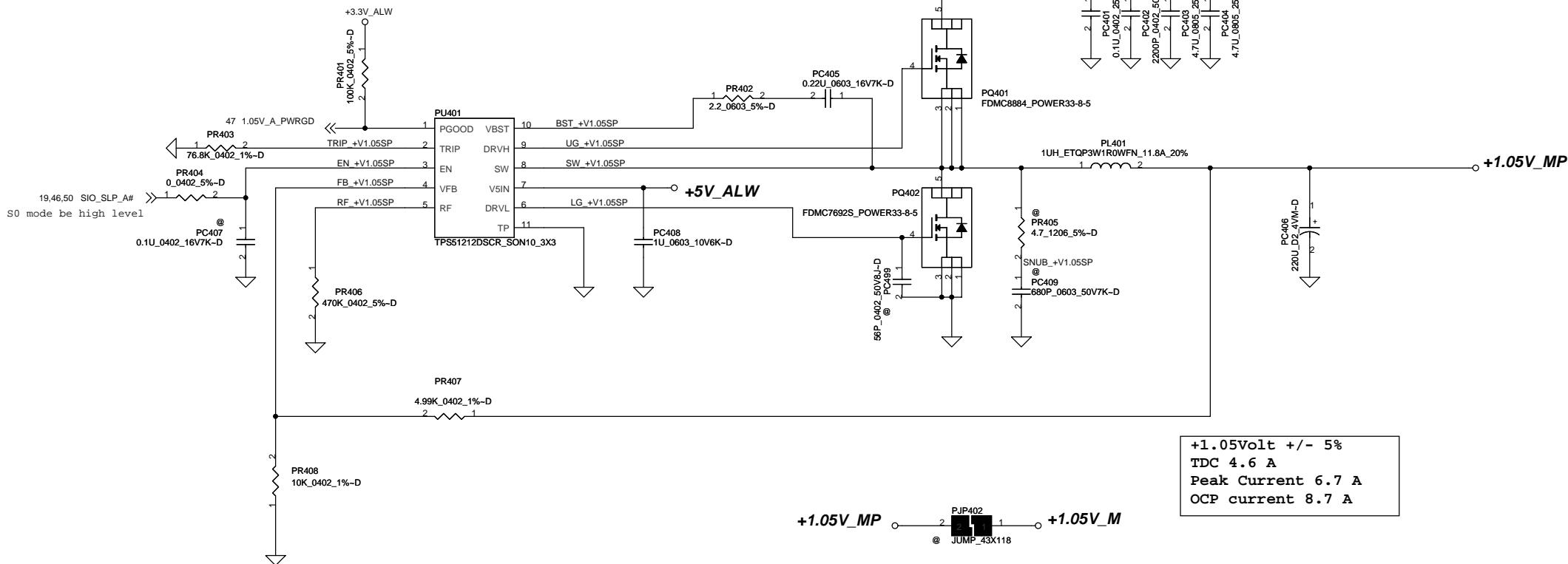


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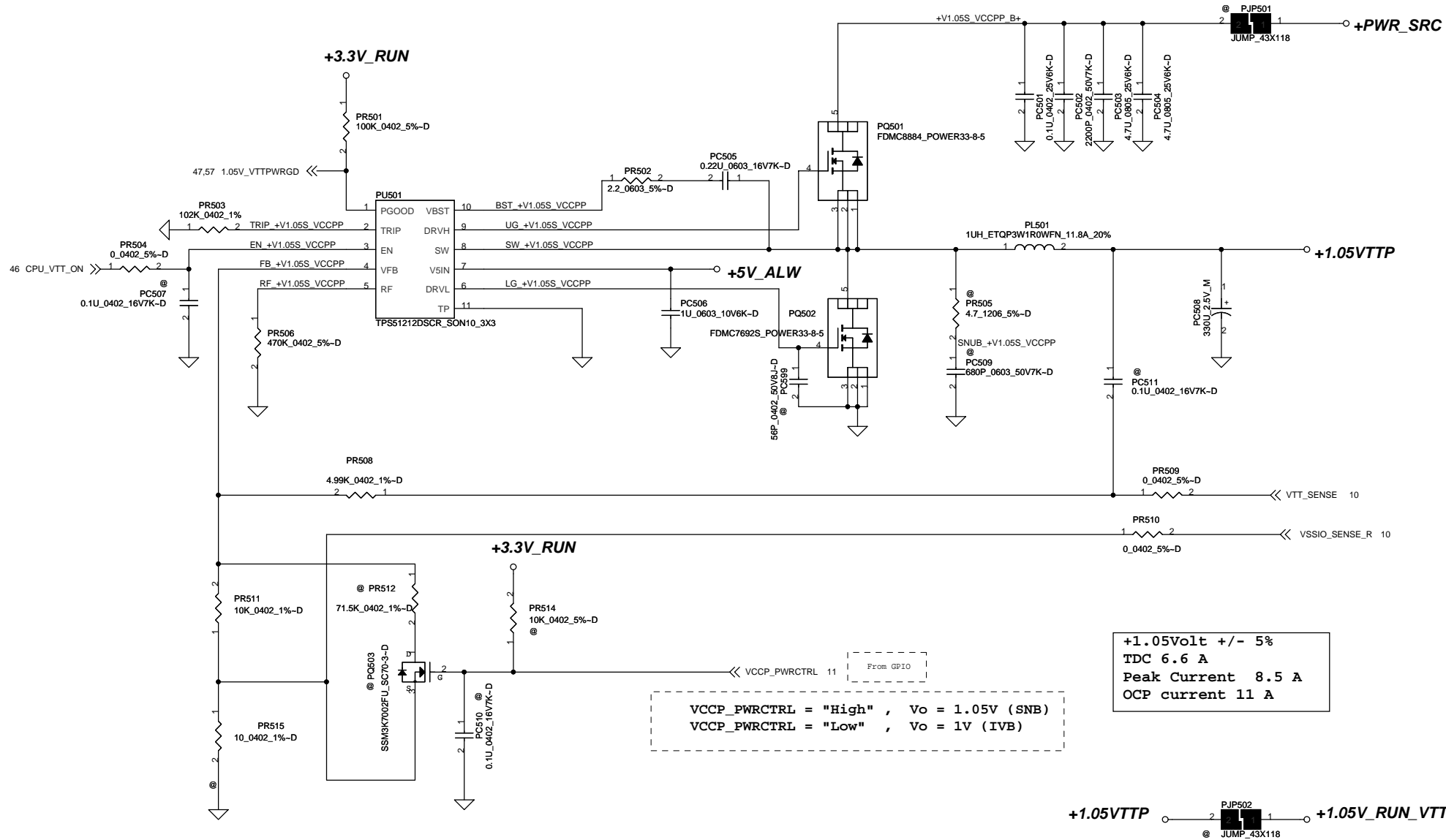


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+1.05V_M		
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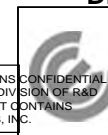


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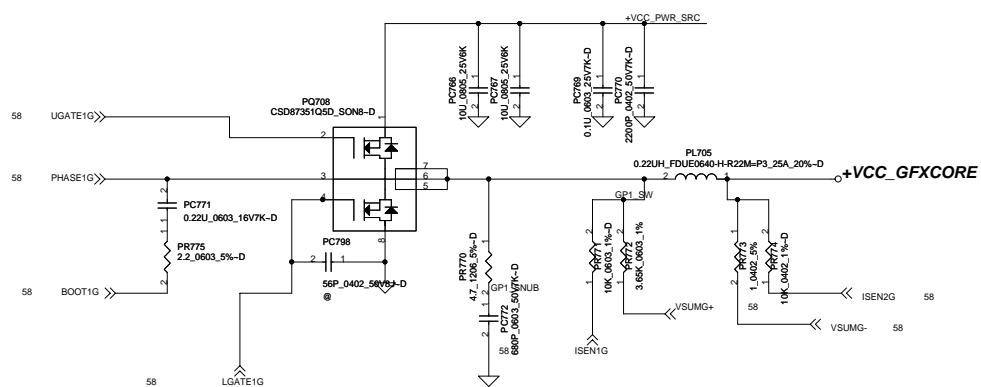
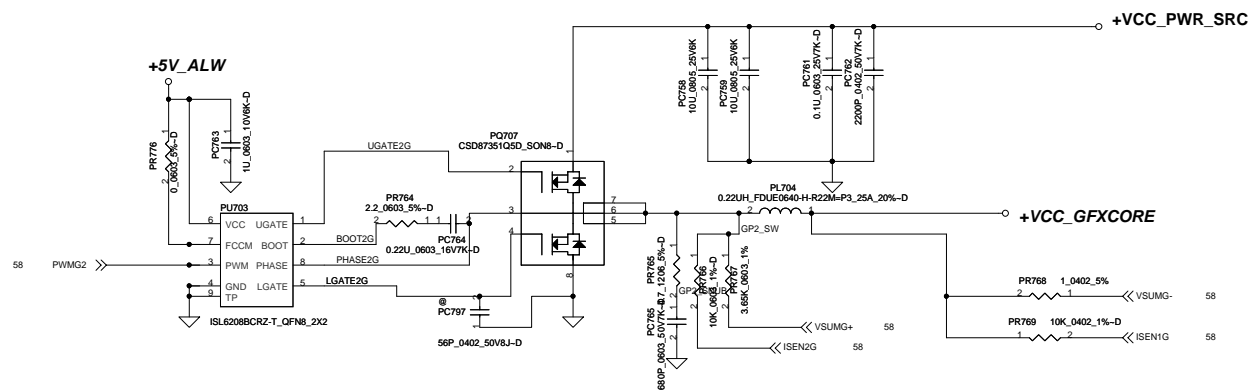
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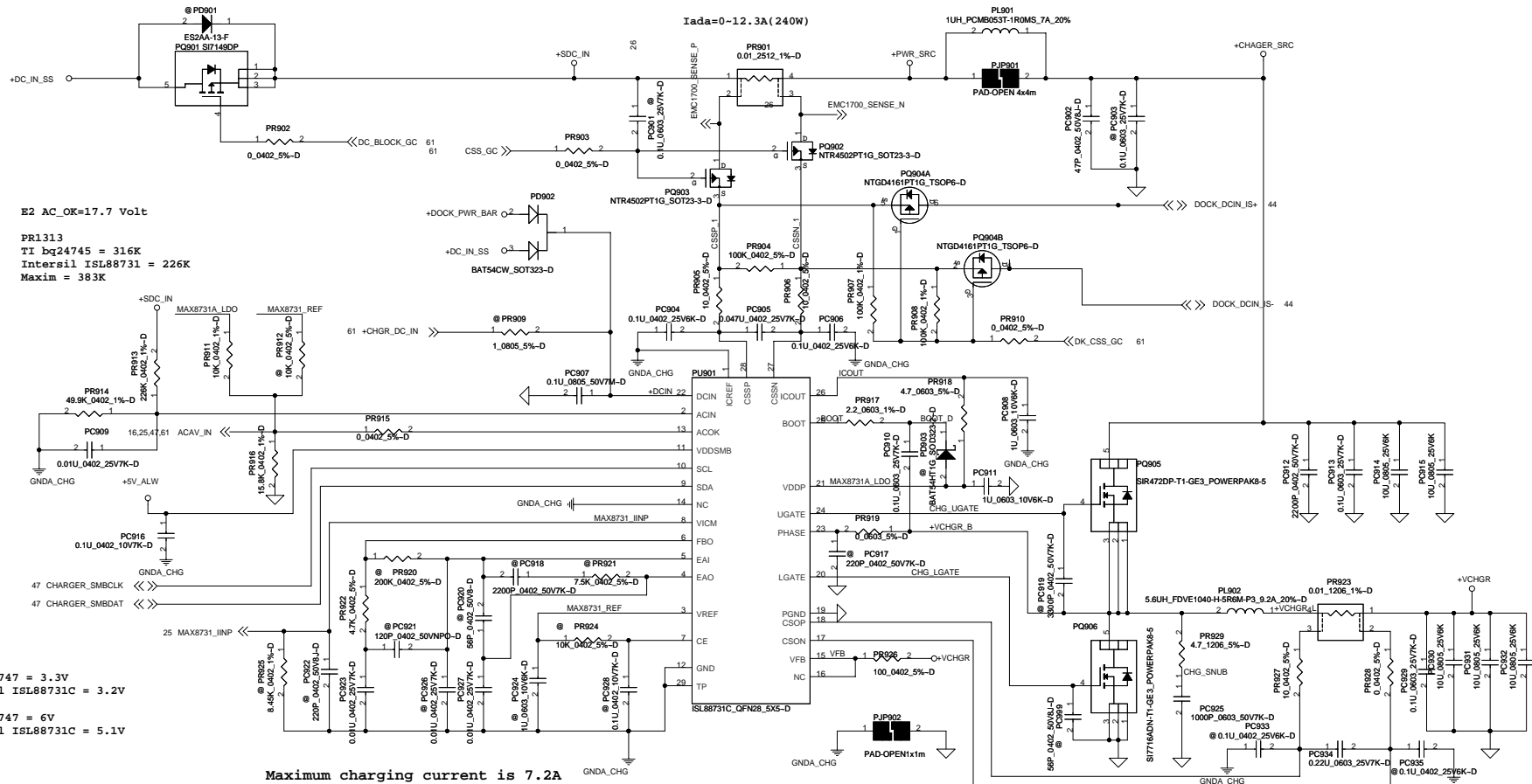
VCC_GFXCORE
TDC 38A
Peak Current 50A
OCP current 57.18A
Load line 3.9



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Adapter Protection Circuit for Turbo Mode

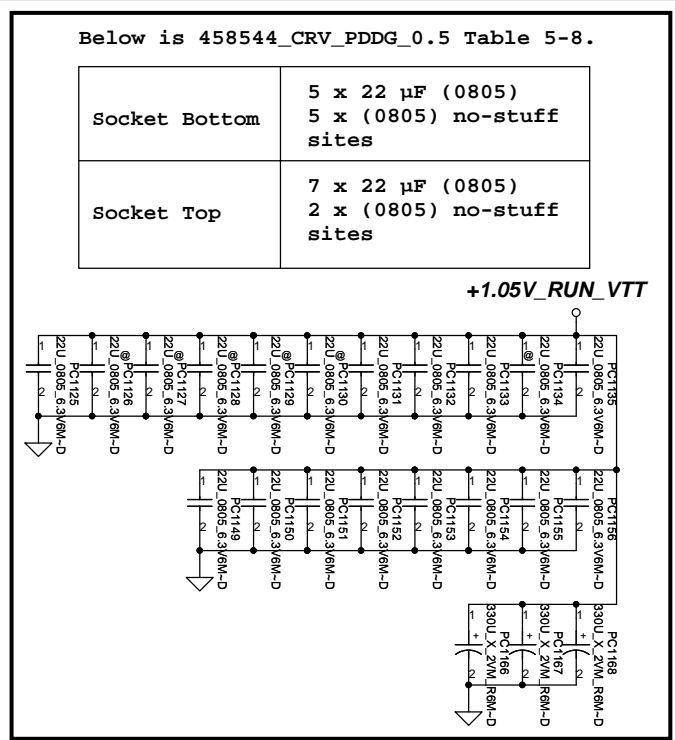
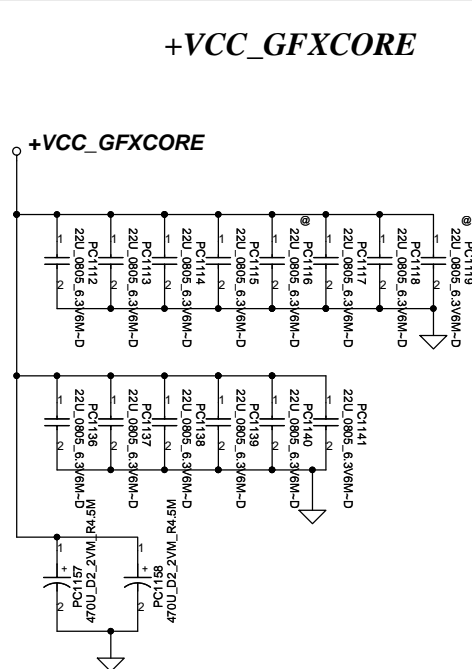
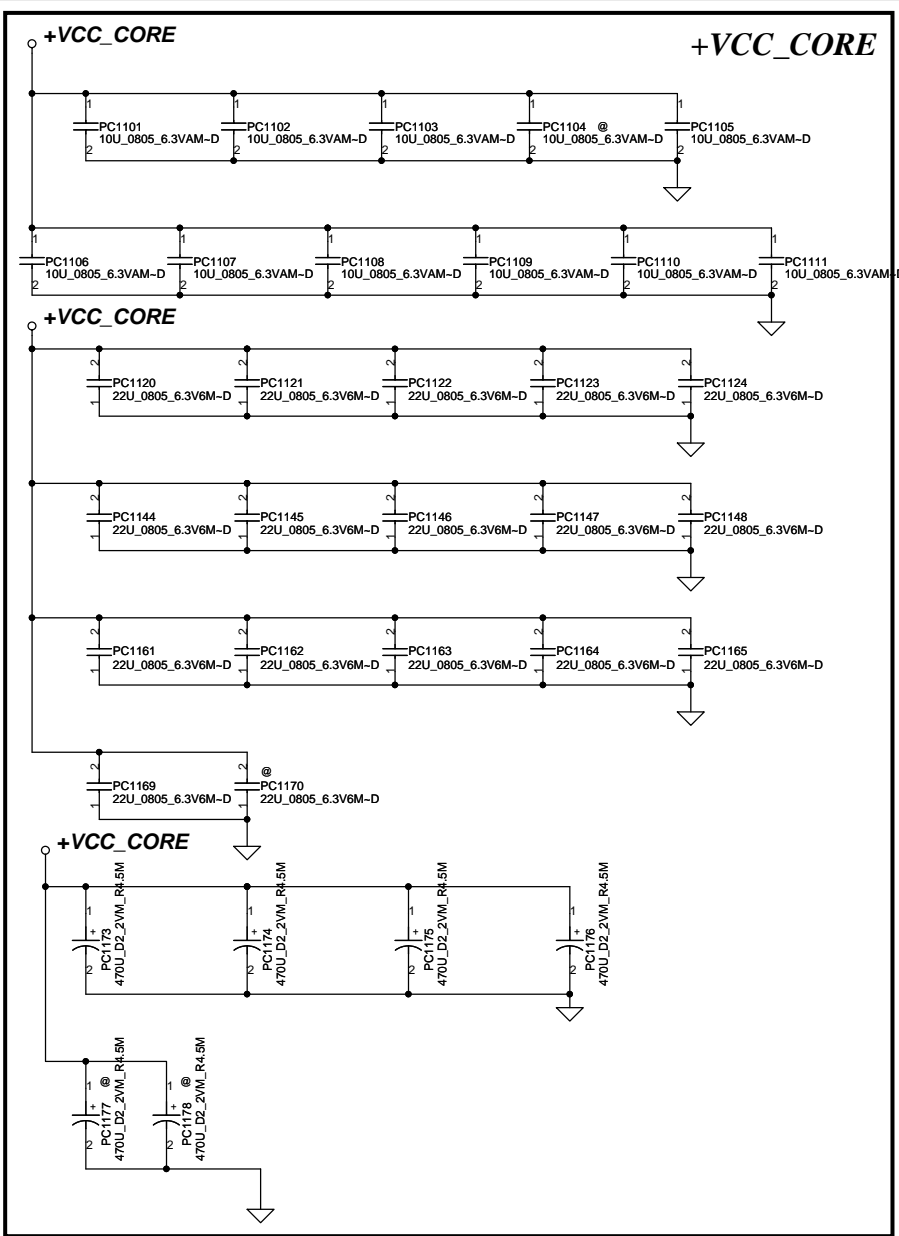
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Charger

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	49	HW	9/23/2011	COMPAL	to meet LED min workable current(2mA).	Change R934,R939,R942,R955,R941 from 2.2kohm to 1.2kohm. R943 from 2.2kohm to 374ohm.	0.2(X01)
2	49	HW	9/23/2011	COMPAL	Breath LED Lose current-limited resistors	Add R956	0.2(X01)
3	26	HW	9/23/2011	DELL	For cost saving	No stuff U5,C17,C363,R1975 U6,C16,C361,R1974	0.2(X01)
4	47	HW	9/23/2011	COMPAL	Code change	U54 change from SA00003TZ2L to SA00003TZ1L	0.2(X01)
5	16	HW	9/23/2011	COMPAL	correct MXM LVDS signals.	Swap CHA and CHB signals on JMXM1.	0.2(X01)
6	32	HW	10/04/2011	COMPAL	Add DOCK DPB DDC signals control circuit.	Stuff C1174,R1532,R1537,R1530,R1539,Q110,Q113	0.2(X01)
7	33	HW	10/04/2011	COMPAL	Add DOCK DPA DDC signals control circuit.1/2	Add C1332,R2151-R2153,R2155-R2157,Q335,Q336	0.2(X01)
8	50	HW	10/04/2011	COMPAL	+3.3V_RUN boot leakage	Pop R929,Q69	0.2(X01)
9	33	HW	10/04/2011	COMPAL	Change the R518 value to meet the PS8336B input high-level voltage.	Change R518 from 100k to 10kohm.	0.2(X01)
10	50	HW	10/04/2011	COMPAL	Solve S4/S5 +MXM_PWR_SRC leakage in DC mode.	Change R940 pin1 connect from +PWR_SRC_S to +PWR_SRC_MXM.	0.2(X01)
11	30	HW	10/05/2011	COMPAL	Due to LVDS and eDP use same connector . It will easy to damage on MB or panel when install wrong 40pin connector for LVDS and eDP	Change eDP pin defined same as LVDS	0.2(X01)
12	30	HW	10/05/2011	COMPAL	Q13 VGS voltage limit of ±20V	Change R162 pin1 connect from +PWR_SRC_S to +3.3V_ALW.	0.2(X01)
13	17,18,47 36	HW	10/05/2011	COMPAL	Crystal EA.	Change C743,C741 from 22pF to 39pF, CH2,CH3 from 15pF to 18pF, CH18,CH19 from 12pF to 10pF, C470 from 33pF to 22pF, C471 from 33pF to 27pF	0.2(X01)
14	46	HW	10/12/2011	COMPAL	Wireless switch needs to be pulled to ALW, Without it being pulled to ALW rail AOAC will not work correct.	Add R2158 let WIRELESS_ON#/OFF pull up to ALW, no stuff R766	0.2(X01)
15	49	HW	10/13/2011	COMPAL	Solve Breath LED flicker when AC in plug and correct Breath LED top and side view work behavior.	Add Q327 and use"MASK_BASE_LEDS#" to control Breath LED top view. use"SVG_LED_MASK#" to control Breath LED side view.	0.2(X01)
16	48	HW	10/13/2011	COMPAL	To meet intel spec:T235(power off)=min40ns). T08a(power on)= max 90ms.	change U4 from RT9801AGE to RT9818A-44GU3,R1622 to 100kohm.add R2159. remove R1649~R1654 pop R1633,non-pop R1623	0.2(X01)
17	44,28,30 45,25,12	ME	10/13/2011	COMPAL	Change connector follow connector list 0913A and 1005A.	Change JDock1 to WD2F144WB5R400,JLVDS1,JEDP1 to 50398-04071-001,JPB1 to 50228-0067N-001. JFAN1 & JFAN2 to 50271-0040N-001, JDIMM1 to 2-2013311-1	0.2(X01)
18	48	HW	10/20/2011	COMPAL	To avoid layout trace width less to 10mil	Add U4.1 net name of +5V_ALW_PCH_R	0.2(X01)
19	28,30	HW	10/20/2011	COMPAL	Avoid JEDP1 and JLVDS1 insert anti burn panel from +BL_PWR_SRC	Q22.2 connector to JEDP1.11	0.2(X01)
20	40	HW	10/25/2011	COMPAL	TPM chip to new version chip due to OS Win8 supported problem	Change U39 TPM solution to new p/n: SA00004WQ10	0.2(X01)
21	44	HW	10/25/2011	COMPAL	Audio not transfer to DP display if play movie when attached external DP display	Add pull down 100K on MXM_DPB_HPD of R2160	0.2(X01)

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22	49	HW	10/25/2011	COMPAL	BT LED will be light when system is in S3/S4/S5	We change R938 PU from +3.3V_RUN to +3.3V_ALW and It can fix this issue.	0.2(X01)
23	50	HW	10/26/2011	COMPAL	For smart card detect failed	For +3.3V_SUS power sequence.Change C767 from 4700pF to 470pF	0.2(X01)
24	50	HW	10/26/2011	COMPAL	For Inrush current issue	Modify +5V_RUN/+3.3V_RUN soft start.Change C777 from 470pF to 2200pF	0.2(X01)
25	49	HW	10/26/2011	COMPAL	Breath LED need to add control schematics	Remove Q327 and modify EC code from PWM Output to GPIO input on ECE5048(GPIOM3/PWM4) which follow E4 solution.	0.2(X01)
26	22	HW	10/26/2011	COMPAL	CRT ripple garbage display issue. 1/2	change LH1 to 1uH inductor.	0.2(X01)
27	39	DFB	10/27/2011	COMPAL	DFB Suggest to relocate L41,L43,L44 from bottom to top side.	In order to trace along the line of the L41,L43,L44 reverse	0.2(X01)
28	49	HW	10/27/2011	COMPAL	Schematic error, let H26, H27,H28,H29 all have two location(H22, H23, H24, H25) in the CAD file	Remove H26,H27,H28,H29	0.2(X01)
29	44	HW	11/01/2011	COMPAL	EMI request,add 33ohm for DOCK DVI signals.	Add R2164~R2179(33ohm) for DOCK DVI port A,B.	0.2(X01)
30	22	HW	11/02/2011	COMPAL	CRT ripple garbage display issue. 2/2	Add CH37 of 10U 0603	0.2(X01)
31	21	HW	11/02/2011	COMPAL	PCH has internal pull up 20k ohm on (GPIO27)	No stuff RH175	0.2(X01)
32	21	HW	11/02/2011	COMPAL	Power saving	RH179 change from 10K to 100K	0.2(X01)
33	33	HW	11/02/2011	COMPAL	EMI request and HDMI EA have verify it.	Pop R451~R456,R458,R459 and non-pop L19,L23~25 R74 change from 4.99k to 5.76K for reduce swing.	0.2(X01)
34	47	HW	11/02/2011	COMPAL	Change board ID to X01	Change R875 to 130K	0.2(X01)
35	50	HW	11/02/2011	COMPAL	Power saving	R935 change from 20K to 100K	0.2(X01)
36	40	HW	11/02/2011	COMPAL	U39.14 internal is empty pin	No stuff C554	0.2(X01)
37	20	HW	11/02/2011	COMPAL	Avoid WWAN noise affect PCI 3,3M CLK.	Add CH21~23 by pass cap.	0.2(X01)
38	39	HW	11/02/2011	COMPAL	For ESD request.	D14,D16 change main source SC30000250L to SC300002F0L	0.2(X01)
39	49	ME	11/03/2011	COMPAL	ME drawing modify	Remove H21 and H10 from 3P3 to 3P0	0.2(X01)
40	44	HW	11/03/2011	COMPAL	For ESD request.	Non-pop D33,D10,D11	0.2(X01)
41	37	HW	11/03/2011	COMPAL	Vendor service issue	Change T156 from P050005A0L(PULSE) to SP050006P0L(TAIMAG)	0.2(X01)
42	33	HW	11/03/2011	COMPAL	Add DOCK DPA DDC signals control circuit.2/2	Add R2154,R2161,R2162,R2163,Q337 but no stuff	0.2(X01)
43	33	HW	11/04/2011	COMPAL	EMI request,add reserve C(3.3pF) for HDMI signals.	Add reserve C1333~C1340(3.3pF) for HDMI signals.	0.2(X01)
44	31	LAYOUT	11/08/2011	COMPAL	Add TEST point for JCRT PIN11.	Add CRT_11 net and test point(T61) for JCRT1.11.	0.2(X01)
45	07	HW	11/08/2011	COMPAL	Avoid Power_SRC trace noise coupling effect to CPU	Add CC92	0.2(X01)
46	26,50	HW	11/09/2011	DELL	For DELL request add Monitor PWR_SRC MXM circuit by HW control	Remove R1973, add PJP78,79 Remove U5,C17,C363,R1975,R1181,R20,U6,C16,C361,R1974,R19 Add U59,PU2,PQ1005,PR14,PR24~31,PC6,PC17~21 and no stuff	0.2(X01)
47	44	HW	11/11/2011	COMPAL	For DP EA consider	Change R2164~R2179(33ohm) to 0ohm	0.2(X01)
48	39	HW	11/11/2011	COMPAL	For USB EA JUSB1 ,Need to pop R24/R15/R18 JUSB2 ,Need to pop R33/R27/R29	Pop R15,R27	0.2(X01)

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